NTE1177
Integrated Circuit
TV Luminance Processor

Description:
The NTE1177 is a monolithic silicon integrated circuit in a 14–Lead DIP type package that performs the luminance processing functions of amplification; contrast, brightness and peaking control; blanking; and black-level clamping.

Features:
- Black–Level Clamping
- Linear DC Controls for Brightness, Contrast, and Peaking
- Horizontal and Vertical Blanking
- Operates with Standard or Tapped Delay Line

Absolute Maximum Ratings:
DC Supply Current (Into Pin13, Note 1), \( V_{CC} \) ............................................ 59.5mA
Device Dissipation (Up to \( T_A = +55^\circ C \), Note 1), \( P_D \) ............................................ 750mW
Derate Above 55\(^\circ\)C ............................................ 7.9mW/\(^\circ\)C
Operating Ambient Temperature Range, \( T_{opr} \) ............................................. –40\(^\circ\) to +85\(^\circ\)C
Storage Temperature Range, \( T_{stg} \) ............................................. –65\(^\circ\) to +150\(^\circ\)C
Lead Temperature (During Soldering, 1/16” from case, 10sec max), \( T_L \) ........................................ +265\(^\circ\)C

Note 1. Although the NTE1177 is rated for maximum dissipation of 750mW, it is recommended that the current into Pin13 be limited by external circuit resistance to 39mA for a typical voltage at Pin13 of 11.8V.

Electrical Characteristics: \( (T_A = +25^\circ C \) unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
<th>S5</th>
<th>S6</th>
<th>S7</th>
<th>S8</th>
<th>S9</th>
<th>S10</th>
<th>S11</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage at Pin13</td>
<td>( V_{13} )</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>11.0</td>
<td>11.8</td>
<td>13.2</td>
<td>V</td>
</tr>
<tr>
<td>Quiescent Voltage</td>
<td>( V_{4} )</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>3.3</td>
<td>4.0</td>
<td>5.7</td>
<td>V</td>
</tr>
<tr>
<td>Quiescent Voltage</td>
<td>( V_{7} )</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>7.1</td>
<td>7.7</td>
<td>8.3</td>
<td>V</td>
</tr>
<tr>
<td>Current Into Pin13 Pin13 Connected to +11V</td>
<td>( I_{13} )</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>10</td>
<td>19</td>
<td>30</td>
<td>mA</td>
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</table>
## Electrical Characteristics (Cont’d)

(T_A = +25°C unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Switch Numbers</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>Dynamic Characteristics <em>(Bias Voltage = 5.8V)</em></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>Wide–Band Gain (Note 2)</td>
<td>1 1 1 2 1 2 1 1 2 1</td>
<td></td>
<td>6.0</td>
<td>8.3</td>
<td>11.0</td>
<td>dB</td>
</tr>
<tr>
<td>Contrast Gain Reduction (Note 3)</td>
<td>1 1 1 2 1 2 1 1 2 2 1</td>
<td></td>
<td>27</td>
<td>30</td>
<td>–</td>
<td>dB</td>
</tr>
<tr>
<td>Peaking Gain (Note 2)</td>
<td>1 1 2 2 1 2 1 1 2 1</td>
<td></td>
<td>15.0</td>
<td>18.4</td>
<td>22.0</td>
<td>dB</td>
</tr>
<tr>
<td>Peaking Gain Reduction (Note 4)</td>
<td>1 2 1 2 1 2 1 1 2 1</td>
<td></td>
<td>16</td>
<td>18</td>
<td>–</td>
<td>dB</td>
</tr>
<tr>
<td>Max. Intermodulation Distortion 2V (Note 5)</td>
<td>1 – 1 1 1 2 – 2 1 2 1</td>
<td></td>
<td>–</td>
<td>20</td>
<td>–</td>
<td>%</td>
</tr>
<tr>
<td>3V (Note 6)</td>
<td>1 – 1 1 1 2 – 2 1 2 1</td>
<td></td>
<td>–</td>
<td>40</td>
<td>–</td>
<td>%</td>
</tr>
</tbody>
</table>

Note 2. Set 50kHz generator for 100mV<sub>P-P</sub>. Adjust R1 Peaking Control for minimum setting. Measure wide–band gain at Pin7.

Note 3. Set 50kHz generator for 100mV<sub>P-P</sub>. Adjust R1 for minimum setting. Measure contrast gain reduction at Pin7.

Note 4. Set 50kHz generator for 100mV<sub>P-P</sub>. Adjust R1 for maximum setting. Measure peaking gain reduction at Pin7.

Note 5. Adjust R1 for minimum setting. With S2 at switch position 1 and S7 at switch position 3, set 50kHz generator for 2V<sub>P-P</sub>. Then with S2 at switch position 2, set 1MHz generator for 100mV<sub>P-P</sub>. Then with S7 at switch position 2, measure downward modulation of the 1MHz signal due to the 50kHz signal.

Note 6. Repeat step 5 except that the 50kHz generator must be set at 3V<sub>P-P</sub>.

### Pin Connection Diagram

- Video Input: 1
- Peaking Input: 2
- Peaking Input: 3
- Video Output: 4
- Substrate GND: 5
- Clamp Inhibit: 6
- Clamped Video Out: 7
- N.C.: 14
- Shunt Regulator and Bypass: 13
- Clamp Inhibit Input: 12
- Peaking Control: 11
- Contrast Control: 10
- Blanking Input: 9
- Brightness Control: 8

Dimensions:
- .785 (19.95) Max
- .300 (7.62)
- .200 (5.08) Max
- .099 (2.5) Min
- .600 (15.24)
- .100 (2.45)