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NTE1475
Integrated Circuit
CMOS, Phase–Locked Loop (PLL) Frequency Synthesizer for CB

Features:
- Built–in high speed programmable divider for direct PLL system
- PLL out–of–lock output available to inhibit transmittion.
- Instantaneous call capability of channel 9 and 19.
- Built–in detecting circuit of mis–program
- Built–in amplifier for crystal oscillator
- Built–in amplifier for active low–pass filter.
- BCD code channel selection. (Pull–down resistors included)

Absolute Maximum Ratings: (T_A = +25°C unless otherwie specified)

Maximum Supply Voltage, V_{DD}max . . . . . –0.3 to +8.0V
Maximum Input Voltage, V_{IN}max . . . . . –0.3 to V_{DD} +0.3V
Maximum Output Voltage ($\overline{MC}$, $\overline{LM}$, A_{OUT}, Output Off), $V_{OUT(1)}$ . . . . . –0.3 to +10.0V
Maximum Output Voltage (PD_{OUT}, Output Off), $V_{OUT(2)}$ . . . . . –0.3 to V_{DD} + 0.3V
Maximum Output Current ($\overline{MC}$, $\overline{LM}$), $I_{OUT\ (1)}$ . . . . . 0 to 15mA
Maximum Output Current (A_{OUT}), $I_{OUT\ (2)}$ . . . . . 0 to 2.5mA
Allowable Power Dissipation, $P_D$max (T_A = +70°C) 300mW
Operating Temperature Range, T_{opg} . . . . . –30° to +70°C
Storage Temperature Range, T_{stg} . . . . . –40° to +125°C

Allowable Operating Ranges: (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	T_A = –30° to +70°C	5.0	6.0	7.0	V
Output Voltage	V_{OUT}	$\overline{MC}$, $\overline{LM}$, A_{OUT}, Output Off	0	–	9.0	V
Input Amplitude	$V_{IN\ (1)}$	X_{IN}, $f_{IN\ (1)}$ = 10.25MH_Z, Note 1	1.0	–	0.9V_{DD}	$V_{p–p}$
	$V_{IN\ (2)}$	P_{IN}, $f_{IN\ (2)}$ = 20MH_Z, Note 1	1.0	–	0.9V_{DD}	$V_{p–p}$
Input Frequency	$f_{IN\ (1)}$	X_{IN}, $V_{IN\ (1)}$ = 1.0$V_{p–p}$, Note 1	1.0	–	10.25	MH_Z
	$f_{IN\ (2)}$	P_{IN}, $V_{IN\ (2)}$ = 1.0$V_{p–p}$, Note 1	1.0	–	20	MH_Z
Input “H” Level Voltage	V_{IH}	D1 to D6, $\overline{T}$/R, CH9, CH19	V_{DD}–0.8	–	–	V
Input “L” Level Voltage	V_{IL}	D1 to D6, $\overline{T}$/R, CH9, CH19	–	–	0.8	V

Note 1. Sinusoidal wave, capacitive coupling, T_A = –30° to +70°C

Electrical Characteristics: (T_A = +25°C, V_{DD} = 5V to 7V unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input “H” Level Current	$I_{IH\ (1)}$	X_{IN}, P_{IN}, V_{IN} = V_{DD}	–	–	8.0	µA
Input “L” Level Current	$I_{IL\ (1)}$	X_{IN}, P_{IN}, V_{IN} = V_{SS}	–	–	8.0	µA
Feedback Resistance	R_F	X_{IN}, P_{IN}	–	3.0	–	MΩ
Input Threshold Voltage	V_{th}	X_{IN}, P_{IN}	–	1/2 V_{DD}	–	V
Input “H” Level Current	$I_{IH\ (2)}$	D1 to D6, CH9, CH19, V_{IN} = V_{DD}	60	180	500	µA
Input Floating Voltage	$V_{IF\ (1)}$	D1 to D6, CH9, CH19, Input pins open	–	–	0.2	V
Input “L” Level Current	$I_{IL\ (2)}$	$\overline{T}$/R, V_{IN} = V_{SS}	40	140	400	µA
Input Floating Voltage	$V_{IF\ (2)}$	$\overline{T}$/R, Input pin open	V_{DD}–0.2	–	–	V
Input “H” Level Current	$I_{IH\ (3)}$	A_{IN}, V_{IN} = V_{DD}	–	0.01	–	nA
Input “L” Level Current	$I_{IL\ (3)}$	A_{IN}, V_{IN} = V_{SS}	–	0.01	–	nA
“H” Level 3–State Leak Current	I_{OFFH}	PD_{OUT}, V_{OUT} = V_{DD}	–	0.01	–	nA
“L” Level 3–State Leak Current	I_{OFFL}	PD_{OUT}, V_{OUT} = V_{SS}	–	0.01	–	nA
Output “H” Level Voltage	$V_{OH\ (1)}$	PD_{OUT}, I_{OUT} = 0.3mA	V_{DD}–1.0	–	–	V
Output “L” Level Voltage	$V_{OL\ (1)}$	PD_{OUT}, I_{OUT} = 0.3mA	–	–	1.0	V
Output “H” Level Voltage	$V_{OH\ (2)}$	X_{OUT}, I_{OUT} = 0.5mA	–	V_{DD}–0.35	–	V
Output “L” Level Voltage	$V_{OL\ (2)}$	X_{OUT}, I_{OUT} = 0.5mA	–	0.35	–	V
Output “L” Level Voltage	$V_{OL\ (3)}$	A_{OUT}, I_{OUT} = 0.5mA	–	–	0.3	V
Output Off Leak Current	$I_{OFF\ (1)}$	A_{OUT}, V_{OUT} = 9V	–	–	3.0	µA
Output “L” Level Voltage	$V_{OL\ (4)}$	$\overline{MC}$, $\overline{LM}$, I_{OUT} = 15mA	–	–	1.1	V
Output Off Leak Current	$I_{OFF\ (2)}$	$\overline{MC}$, $\overline{LM}$, V_{OUT} = 9V	–	–	5.0	µA
Current Dissipation	I_{DD}	$f_{IN\ (1)}$ = 10.25MHz, $f_{IN\ (2)}$ = 20MHz, $V_{IN\ (1)}$ = $V_{IN\ (2)}$ = 1.0V_{p-p}, A_{IN} = V_{SS}, D1 = V_{DD}, Other pins open, Number of frequency	–	10	20	mA

Pin Connection Diagram