ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089

NTE1749
Integrated Circuit
Push–Pull Four Channel Driver

Description:

The NTE1749 is a quad push–pull driver capable of delivering output currents to 1A per channel. Each channel is controlled by a TTL–compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Features:

- Output Current 1A Per Channel
- Peak Output Current 2A Per Channel (Non Repetitive)
- Inhibit Facility
- High Noise Immunity
- Separate Logic Supply
- Overtemperature Protection

Absolute Maximum Ratings:

Supply Voltage, V_S 36V
Logic Supply Voltage, V_{SS} 36V
Input Voltage, V_I 7V
Inhibit Voltage, V_{inh} 7V
Peak Output Current (Non–Repetitive, t = 5ms), I_O 2A
Total Power Dissipation ($T_{ground–pins}$ = +80°C), P_D 5W
Operating Junction Temperature Range, T_J . . . . . –40° to +150°C
Storage Temperature Range, T_{stg} . . . . . –40° to +150°C
Maximum Thermal Resistance, Junction–to–Case R_{thJC} . . . . . 14°C/W
Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 80°C/W

Electrical Characteristics: (Per Channel, V_S = 24V, V_{SS} = 5V, T_A = +25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_S		V_{SS}	–	36	V
Logic Supply Voltage	V_{SS}		4.5	–	36	V
Total Quiescent Supply Current	I_S	V_i = L, I_O = 0, V_{inh} = H	–	2	6	mA
		V_i = H, I_O = 0, V_{inh} = H	–	16	24	mA
		V_{inh} = L	–	–	4	mA
Total Quiescent Logic Supply Current	I_S	V_i = L, I_O = 0, V_{inh} = H	–	44	60	mA
		V_i = H, I_O = 0, V_{inh} = H	–	16	24	mA
		V_{inh} = L	–	16	24	mA
Input Low Voltage	V_{IL}		–0.3	–	1.5	V
Input High Voltage	V_{IH}	$V_{SS} \le 7V$	2.3	–	V_{ss}	V
		$V_{SS} > 7V$	2.3	–	7	V
Low Voltage Input Current	I_{IL}	V_{IL} = 1.5V	–	–	–10	µA
High Voltage Input Current	I_{IH}	$2.3V \le V_{IH} \le V_{SS} – 0.6V$	–	30	100	µA
Inhibit Low Voltage	V_{inhL}		–0.3	–	1.5	V
Inhibit High Voltage	V_{inhH}	$V_{SS} \le 7V$	2.3	–	V_{ss}	V
		$V_{ss} > 7V$	2.3	–	7	V
Low Voltage Inhibit Current	I_{inhL}	V_{inhL} = 1.5V	–	–30	100	µA
High Voltage Inhibit Current	I_{IHhH}	$2.3V \le V_{inhH} \le V_{SS} –0.6V$	–	–	±10	µA
Source Output Saturation Voltage	V_{CEsatH}	I_O = –1A	–	1.4	1.8	V
Sink Output Saturation Voltage	$V_{CEsat\ L}$	I_O = 1A	–	1.2	1.8	V
Rise Time	t_r	0.1 to 0.9 V_o	–	250	–	ns
Fall Time	t_f	0.9 to 0.1 V_o	–	250	–	ns
Turn–On Delay Time	t_{on}	0.5 V_i to 0.5 V_o	–	750	–	ns
Turn–Off Delay Time	t_{off}	0.5 V_i to 0.5 V_o	–	200	–	ns

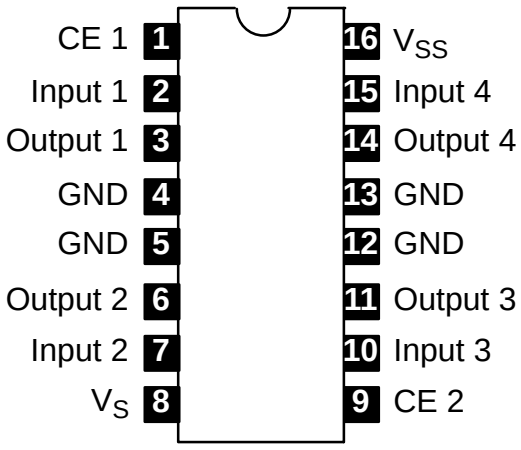
Truth Table

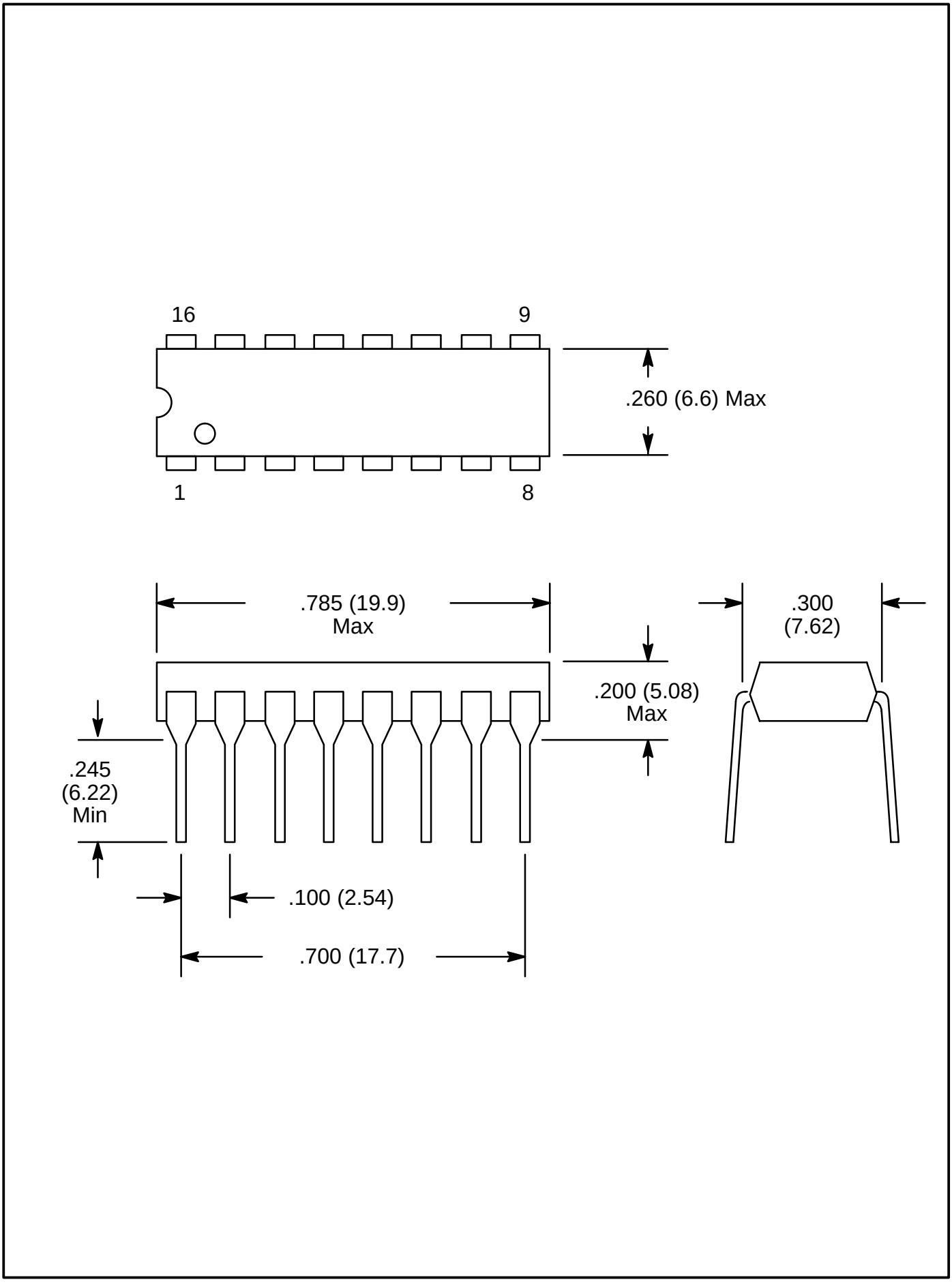
V_i (Each Channel)	V_o	V_{inh} (Note 2)
H	H	H
L	L	H
H	X (Note 1)	L
L	X (Note 1)	L

Note 1. High Output Impedance

Note 2. Relative to the Considerate Channel

Pin Connection Diagram




16
9
.260 (6.6) Max
1
8
.785 (19.9)
Max
.200 (5.08)
Max
.300
(7.62)
.245
(6.22)
Min
.100 (2.54)
.700 (17.7)