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NTE1786
Integrated Circuit
Frequency Lock Loop (FLL)
Tuning & Control Circuit

Description:

The NTE1786 is an integrated circuit in a 24–Lead DIP type package that provides closed–loop digital tuning of TV receivers, with or without AFC, as required. This device also controls up to 4 analog functions, 4 general purpose I/O ports and 4 high–current outputs for tuner band selection.

Features:

- Combined Analog and Digital Circuitry Minimizes the Number of Additional Interfacing Components Required
- Frequency Measurement with Resolution of 50kHz
- Selectable Prescaler Divisor of 64 or 256
- 32V Tuning Voltage Amplifier
- 4 High–Current Outputs for Direct Band Selection
- 4 Static Digital–to–Analog Convertors (DACs) for Control of Analog Functions
- 4 General Purpose Input/Output (I/O) Ports
- Tuning with Control of Speed and Direction
- Tuning with or without AFC
- Single–Pin, 4MHz On–Chip Oscillator
- I^2C Bus Slave Transceiver

Applications:

- TV Receivers
- Satellite Receivers
- CATV Converters

Absolute Maximum Ratings:

Supply Voltage Ranges,

Pin13, V_{CC1} . . . . . –0.3 to +18V
Pin19, V_{CC2} . . . . . –0.3 to +18V
Pin14, V_{CC3} . . . . . –0.3 to +36V

Absolute Maximum Ratings (Cont'd):

Input/Output Voltage Ranges,

Pin2, V_{SDA} . . . . . –0.3 to +18V
Pin3, V_{SCL} . . . . . –0.3 to +18V
Pin4 to Pin7, V_{P2X} . . . . . –0.3 to +18V
Pin8 & Pin9 (Note 1), V_{AFC+}, V_{AFC-} . . . . . –0.3 to V_{CC1}
Pin10, V_{TI} . . . . . –0.3 to V_{CC1}
Pin12 (Note 2), V_{TUN} . . . . . –0.3 to V_{CC3}
Pin15 to Pin18 (Note 2), V_{P1X} . . . . . –0.3 to V_{CC2}
Pin20 (Note 1), V_{FDIV} . . . . . –0.3 to V_{CC1}
Pin21, V_{OSC} . . . . . –0.3 to +5V
Pin1, Pin22 to Pin24 (Note 1), V_{DACX} . . . . . –0.3 to V_{CC1}

Total Power Dissipation, P_{TOT} 1000mW
Operating Ambient Temperature Range, T_A . . . . . –20° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Pin voltage may exceed supply voltage if current is limited to 10mA.
Note 2. Pin voltage must not exceed 18v but may exceed V_{CC2} of current is limited to 200mA.

DC and AC Electrical Characteristics: (T_A = +25°C, V_{CC1}, V_{CC2}, V_{CC3} at typical voltages unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC1}		10.5	12.0	13.5	V
	V_{CC2}		4.7	13.0	16.0	V
	V_{CC3}		30	32	35	V
Supply Current (No Outputs Loaded)	I_{CC1}		18	30	45	mA
	I_{CC2}		0	–	0.1	mA
	I_{CC3}		0.2	0.6	2.0	mA
Additional Supply Currents (A)	I_{CC2A}	Note 3	–2	–	I_{OHP1X}	mA
	I_{CC3A}	Note 3	0.2	–	2.0	mA
Total Power Dissipation	P_{TOT}		–	380	–	mW
Operating Ambient Temperature	T_A		–20	–	+70	°C
I²C Bus Inuts SDA Input (Pin2); SCL Input (Pin3)						
Input Voltage, HIGH	V_{IH}	Note 4	3	–	V_{CC}–1	V
Input Voltage, LOW	V_{IL}		–0.3	–	1.5	V
Input Current, HIGH	I_{IH}	Note 4	–	–	10	µA
Input Current, LOW	I_{IL}		–	–	10	µA
I²C Bus Outputs SDA Output (Pin2, Open Collector)						
Output Voltage, LOW	V_{OL}	I_{OL} = 3mA	–	–	0.4	V
Maximum Output Sink Current	I_{OL}		–	5	–	mA
Open–Collector I/O Ports P20, P21, P22, P23 (Pin4 to Pin7, Open Collector)						
Input Voltage, HIGH	V_{IH}		2	–	16	V
Input Voltage, LOW	V_{IL}		–0.3	–	0.8	V
Input Current, HIGH	I_{IH}		–	–	25	µA
Input Current, LOW	I_{IL}		–	–	25	µA
Output Voltage, LOW	V_{OL}	I_{OL} = 2mA	–	–	0.4	V
Maximum Output Sink Current	I_{OL}		–	4	–	mA

Note 3. For each band–select output which is programmed at logic 1, sourcing a current I_{OOP1X}, the additional supply currents (A) shown must be added to I_{CC2} and I_{CC3}, respectively.
Note 4. If V_{CC1} < 1V, the input current is limited to 10µA at input voltages up to 16V.

DC and AC Electrical Characteristics (Cont'd): (T_A = +25°C, V_{CC1}, V_{CC2}, V_{CC3} at typical voltages unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AFC Amplifier Inputs AFC+, AFC– (Pin8, Pin9)						
Transconductance for Input Voltages up to 1V Differential	g00	AFCS1: 0, AFCS2: 0	100	250	800	nA/V
	g01	AFCS1: 0, AFCS2: 1	15	25	35	µA/V
	g10	AFCS1: 1, AFCS2: 0	30	50	70	µA/V
	g11	AFCS1: 1, AFCS2: 1	60	100	140	µA/V
Tolerance of Transconductance Multiplying Factor (2, 4, or 8) when Correction–in–Band is Used	ΔM_g		–20	–	+20	%
Input Offset Voltage	V_{IOFF}		–75	–	+75	mV
Common–Mode Input Voltage	V_{COM}		3	–	V_{CC1}–2.5	V
Common–Mode Rejection Ratio	CMRR		–	50	–	dB
Power Supply (V_{CC1}) Rejection Ratio	PSRR		–	50	–	dB
Input Current	I_I		–	–	500	nA
Tuning Voltage Amplifier Input TI, Output TUN (Pin10, Pin12)						
Maximum Output Voltage	V_{TUN}	I_{LOAD} = ±2.5mA	V_{CC3}–1.6	–	V_{CC3}–0.4	V
Maximum Output Voltage	V_{TM00}	I_{LOAD} = ±2.5mA, VTMI1: 0, VTMI0: 0	300	–	500	mV
	V_{TM10}	I_{LOAD} = ±2.5mA, VTMI1: 1, VTMI0: 0	450	–	650	mV
	V_{TM11}	I_{LOAD} = ±2.5mA, VTMI1: 1, VTMI0: 1	650	–	900	mV
Maximum Output Source Current	$-I_{TUNH}$		2.5	–	8.0	mA
Maximum Output Sink Current	I_{TUNL}		–	40	–	mA
Input Bias Current	I_{TI}		–5	–	+5	nA
Power Supply (V_{CC3}) Rejection Ratio	PSRR		–	60	–	dB
Minimum Charge IT to Tuning Voltage Amplifier	CH_{00}	TUHN1: 0, TUHN0: 0	0.4	1.0	1.7	µA/V
	CH_{01}	TUHN1: 0, TUHN0: 1	4	8	14	µA/V
	CH_{10}	TUHN1: 1, TUHN0: 0	15	30	48	µA/V
	CH_{11}	TUHN1: 1, TUHN0: 1	130	250	370	µA/V
Tolerance of Charge (or ΔV_{TUN}) Multiplying Factor when COIB and/or TUS are Used	ΔCH		–20	–	+20	%
Maximum Current I into Tuning Amplifier	I_{T00}	TUHN1: 0, TUHN0: 0	1.7	3.5	5.1	µA
	I_{T01}	TUHN1: 0, TUHN0: 1	15	29	41	µA
	I_{T10}	TUHN1: 1, TUHN0: 0	65	110	160	µA
	I_{T11}	TUHN1: 1, TUHN0: 1	530	875	1220	µA
Correction–in–Band						
Tolerance of Correction–in–Band Levels 12V, 18V, and 24V	ΔV_{CIB}		–15	–	+15	%
Band–Select Output Ports P10, P11, P12, P13 (Pin15 to Pin18)						
Output Voltge, HIGH	V_{OH}	$-I_{OH}$ = 50mA, Note 5	V_{CC2}–0.6	–	–	V
Output Voltage, LOW	V_{OL}	I_{OL} = 2mA	–	–	0.4	V

Note 5. At continuous operation the output current should not exceed 50mA. When the output is short–circuited to GND for several seconds the device may be damaged.

DC and AC Electrical Characteristics (Cont'd): (T_A = +25°C, V_{CC1}, V_{CC2}, V_{CC3} at typical voltages unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Band–Select Output Ports (Cont'd) P10, P11, P12, P13 (Pin15 to Pin18)						
Maximum Output Source Current	$-I_{OH}$	Note 5	–	130	200	mA
Maximum Output Sink Current	I_{OL}		–	5	–	mA
FDIV Input (Pin20)						
Input Voltage (Peak–to–Peak Value)	$V_{FDIV}^{P-P)}$	t_{RISE} and $t_{FALL} \le 40$ns	0.1	–	2.0	V
Duty Cycle			40	–	60	%
Maximum Input Frequency	f_{MAX}		14.5	–	–	MHz
Input Impedance	Z_i		–	8	–	kΩ
Input Capacitance	C_I		–	5	–	pF
OSC Input (Pin21)						
Crystal Resistance at Resonance (4MHz)	R_X		–	–	150	Ω
DAC Outputs (Pin1, Pin22 to Pin24)						
Maximum Output Voltage (No Load)	V_{DH}	V_{CC1} = 12V, Note 6	10.0	–	11.5	V
Minimum Output Voltage (No Load)	V_{DL}	V_{CC1} = 12V, Note 6	0.1	–	1.0	V
Positive Value of Smallest Step	ΔV_D	1 Least Significant Bit	0	–	350	mV
Deviation from Linearity			–	–	0.5	V
Output Impedance	Z_D	I_{LOAD} = ±2mA	–	–	70	Ω
Maximum Output Source Current	$-I_{DH}$		–	–	6	mA
Maximum Output Sink Current	I_{DL}		–	8	–	mA
Power–Down Reset						
Maximum Supply Voltage (V_{CC1}) at which Power–Down Reset is Active	V_{PD}		7.5	–	9.5	V
V_{CC1} Rise Time During Power–Up (Up to V_{PD})	t_R		5	–	–	µs
Voltage Level for Valid Module Address						
Voltage Level at P20 (Pin4) for Valid Module Address as a Function of MA1, MA0	V_{VA00}	MA1: 0, MA0: 0	–0.3	–	16	V
	V_{VA01}	MA1: 0, MA0: 1	–0.3	–	0.8	V
	V_{VA10}	MA1: 1, MA0: 0	2.5	–	V_{CC1}–2	V
	V_{VA11}	MA1: 1, MA0: 1	V_{CC1}–0.3	–	V_{CC1}	V

Note 5. At continuous operation the output current should not exceed 50mA. When the output is short–circuited to GND for several seconds the device may be damaged.

Note 6. Values are proportional to V_{CC1}.

Pin Connection Diagram