ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE2128
Integrated Circuit
16K (2048 x 8–Bit) StaticRandom Access Memory (RAM)

Description:

The NTE2128 is a 16,384–bit Random–Access Memory (RAM) device in a 24–Lead DIP type package organized as 2048 words by 8 bits. Using a scaled NMOS technology, its design provides the ease–of–use features associated with non–clocked static memories. This device has a three–state output and offers a standby mode with an attendent 75% savings in power consumption. It features equal access and cycle times and provides an output enable function that eliminates the need for external bus buffers.

Features:

- Scaled NMOS Technology
- Completely Static Memory: No Clock, No Refresh
- Equal Access and Cycle Times
- Single +5V Power Supply
- Automatic Power–Down
- All Inputs and Outputs Directly TTL Compatible
- Common I/O Capability
- $\overline{OE}$ Eliminates Need for External Bus Buffers
- Three–State Outputs
- Low Power Dissipation in Standby Mode
- Access Time: 150ns
- R/W Cycle Time: 150ns

Absolute Maximum Ratings: (Note 1)

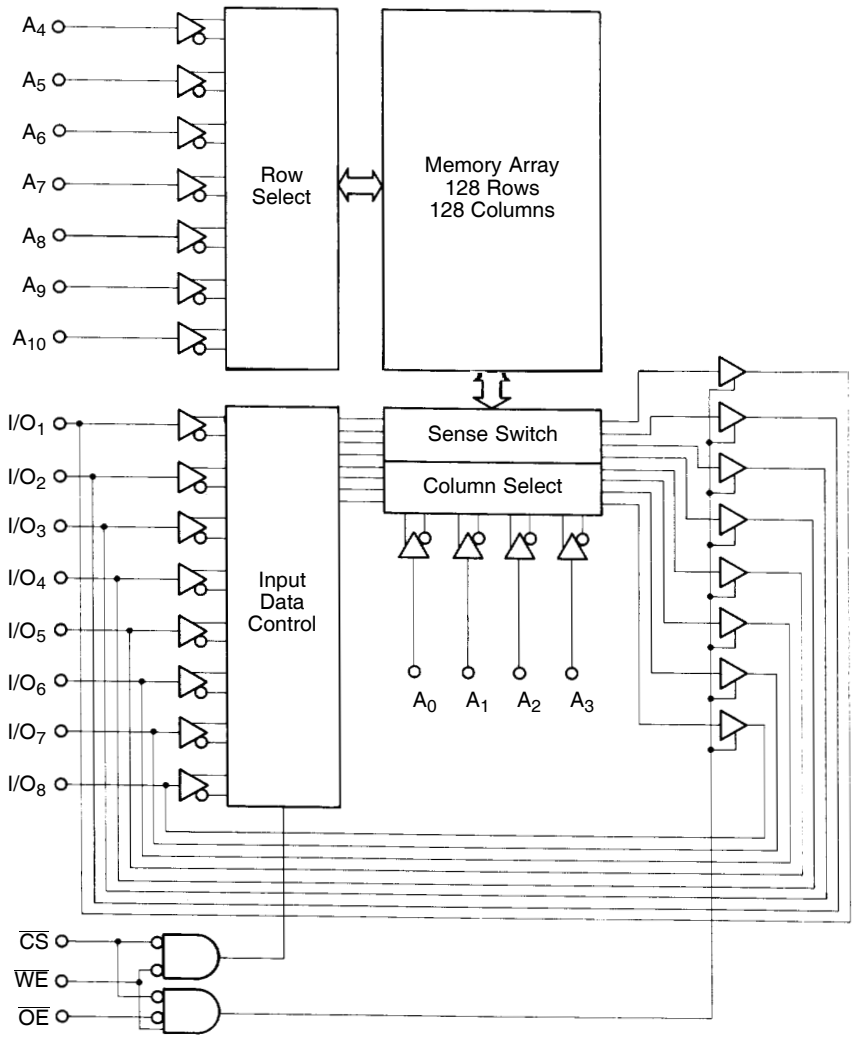
Voltage on Any Pin with Respect to GND . . . . . –1.5V to +7V
DC Output Current, I_O 20mA
Power Dissipation, P_D 1W
Storage Temperature Range, T_{stg} . . . . . –55° to +125°C
Temperature Under Bias . . . . . –10° to +85°C

Note 1. Exposing the device to stresses above those listed in the “Absolute Maximum Ratings” could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
H	X	X	Not Selected	High−Z	Standby
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	L	Write	D_{IN}	Active

Block Diagram



Capacitance: (T_A = +25°C, f = 1MHz, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	5	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	–	7	pF

Note 2. This parameter is sampled and not 100% tested.

DC Characteristics: (T_A = 0° to +70°C, V_{CC} = 5V ±10% unless otherwise specified)

Parameter	Symbol	Test Conditions (Note 3)	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND to V_{CC}	–	–	10	μA
Output Leakage Current	I_{LO}	V_{CC} = Max, $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	–	10	μA
Operating Current	I_{CC}	V_{CC} = Max, $\overline{CS}$ = V_{IL}, Outputs Open	–	–	60	mA
Standby Current	I_{SB}	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}	–	–	15	mA
Input Low Voltage	V_{IL}		–1.5	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	6.0	V
Output Low Voltage	V_{OL}	I_{OL} = 4mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = 1mA	2.4	–	–	V
Output Short−Circuit Current	I_{OS}	V_{OUT} = GND to V_{CC}	–	70	–	mA

Note 3. Input Pulse Levels: 0.8V to 2.2V
Input Rise and Fall Times: 10ns
Input Timing Reference Levels: 1.5V
Output Timing Reference Levels: 1.5V

AC Characteristics: (T_A = 0° to +70°C, V_{CC} = 5V ±10% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Read Cycle						
Read Cycle Time	t_{RC}	Note 4	150	–	–	ns
Address Access Time	t_{AA}		–	–	150	ns
Chip Select Access Time	t_{ACS}	Note 5	–	–	150	ns
Output Hold from Address Change	t_{OH}		10	–	–	ns
Chip Selection to Output in Low−Z	t_{LZ}	Note 2, Note 6	10	–	–	ns
Chip Deselection to Output in High−Z	t_{HZ}	Note 2, Note 6	–	–	50	ns
Output Enable to Output Valid	t_{OE}		–	–	70	ns
Output Enable to Output in Low−Z	t_{OLZ}	Note 2, Note 6	10	–	–	ns
Output Disable to Output in High−Z	t_{OHZ}	Note 2, Note 6	–	–	50	ns
Chip Selection to Power−Up Time	t_{PU}	Note 2	0	–	–	ns
Chip Deselection to Power−Down Time	t_{PD}	Note 2	–	–	70	ns
Write Cycle						
Write Cycle Time	t_{WC}		150	–	–	ns
Chip Selection to End of Write	t_{CW}		120	–	–	ns
Address Valid to End of Write	t_{AW}		90	–	–	ns
Address Set−Up Time	t_{AS}		0	–	–	ns
Write Pulse Width	t_{WP}	Note 7	80	–	–	ns
Write Recovery Time	t_{WR}		10	–	–	ns
Data Valid to End of Write	t_{DW}		50	–	–	ns
Data Hold Time	t_{DH}		0	–	–	ns
Write Enabled to Output in High−Z	t_{WZ}	Note 2, Note 6	–	–	50	ns
Output Active from End of Write	t_{OW}	Note 2, Note 6	10	–	–	ns

Note 4. All read cycle timings are referrenced from the last valid address to the first transition address.

Note 5. Address valid prior to or coincident with $\overline{CS}$ transition low.

Note 6. Transition is measured ±200mV from steady−state voltage with specified load.

Note 7. If $\overline{CS}$ and $\overline{OE}$ are both low before write enable, $t_{WP} = t_{WZ} + t_{DW}$.

Pin Connection Diagram