

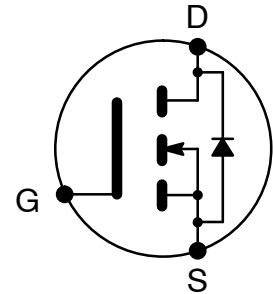


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**NTE2949
 MOSFET
 N-Channel, Enhancement Mode
 High Speed Switch
 TO-220 Full Pack Type Package**

Features:

- Ultra Low Gate Charge
- Periodic Avalanche Rated
- Extreme dv/dt Rated
- High Peak Current Capability
- Improved Transconductance



Absolute Maximum Ratings:

Continuous Drain Current, I_D	
$T_C = +25^\circ\text{C}$	20.7A
$T_C = +100^\circ\text{C}$	13.1A
Pulsed Drain Current (t_p limited by T_{Jmax}), I_{Dpuls}	62.1A
Single Pulse Avalanche Energy ($I_D = 10\text{A}$, $V_{DD} = 50\text{V}$), E_{AS}	690mJ
Repetitive Avalanche Energy (t_{AR} limited by T_{Jmax} , $I_D = 10\text{A}$, $V_{DD} = 50\text{V}$, Not 2), E_{AR}	1mJ
Repetitive Avalanche Current (t_{AR} limited by T_{Jmax}), I_{AR}	20A
Gate-Source Voltage, V_{GS}	
Static	$\pm 20\text{V}$
AC ($f > 1\text{Hz}$)	$\pm 30\text{V}$
Total Power Dissipation ($T_C = +25^\circ\text{C}$), P_{tot}	34.5W
Reverse Diode dv/dt (Note 3), dv/dt	15V/ns
Drain-Source Voltage Slope ($V_{DS} = 480\text{V}$, $I_D = 20.7\text{A}$, $T_J = +125^\circ\text{C}$), dv/dt	50V/ns
Junction Temperature Range, T_J	-55° to $+150^\circ\text{C}$
Storage Temperature Range, T_{stg}	-55° to $+150^\circ\text{C}$
Lead Temperature (wavesoldering, .063" [1.6mm] from case, 10sec), T_{sold}	$+260^\circ\text{C}$
Thermal Resistance, Junction-to-Case, R_{thJC}	3.6K/W
Thermal Resistance, Junction-to-Ambient, R_{thJA}	80K/W

Note 1. Limited only by maximum temperature.

Note 2. Repetitive avalanche causes additional power losses that can be calculated as $P_{AV} = E_{AR} + f$.

Note 3. $I_{SD} \leq I_D$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DClk} = 400\text{V}$, $V_{peak} < V_{(BR)DSS}$, $T_J < T_{Jmax}$, identical low-side and high-side switch.



Electrical Characteristics: ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 0.25mA$	600	–	–	V
Gate–Source Avalanche Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = 0V, I_D = 20A$	–	700	–	V
Gate Threshold Voltage	$V_{GS(th)}$	$I_D = 1000\mu A, V_{GS} = V_{DS}$	2.1	3.0	3.9	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600V, V_{GS} = 0, T_J = +25^\circ\text{C}$	–	0.1	1.0	μA
		$V_{DS} = 600V, V_{GS} = 0, T_J = +100^\circ\text{C}$	–	–	100	μA
Gate–Source Leakage Current	I_{GSS}	$V_{GS} = 30V, V_{DS} = 0V$	–	–	100	nA
Drain–Source ON–State Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 13.1A, T_J = +25^\circ\text{C}$	–	0.16	0.19	Ω
		$V_{GS} = 10V, I_D = 13.1A, T_J = +150^\circ\text{C}$	–	0.43	–	W
Gate Input Resistance	R_G	$f = 1MHz, \text{Open Drain}$	–	0.54	–	W
Transconductance	g_{fs}	$V_{DS} = 2 * I_D * R_{DS(on)max}, I_D = 13.1A$	–	17.5	–	S
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$	–	2400	–	pF
Output Capacitance	C_{oss}		–	780	–	pF
Reverse Transfer Capacitance	C_{rss}		–	50	–	pF
Effective Output Capacitance, Energy Related	$C_{o(er)}$	$V_{GS} = 0V, V_{DS} = 0 \text{ to } 480V, \text{Note 4}$	–	83	–	pF
Effective Output Capacitance, Time Related	$C_{o(tr)}$	$V_{GS} = 0V, V_{DS} = 0 \text{ to } 480V, \text{Note 5}$	–	100	–	pF
Turn–On Delay Time	$t_{d(on)}$	$V_{DD} = 380V, V_{GS} = 0 \text{ to } 13V, I_D = 20.7A$	–	10	–	ns
Rise Time	t_r		–	5	–	ns
Turn–Off Delay Time	$t_{d(off)}$		–	67	100	ns
Fall Time	t_f		–	4.5	12	ns
Gate–Source Charge	Q_{gs}	$V_{DD} = 480V, I_D = 20.7A$	–	11	–	nC
Gate–Drain Charge	Q_{gd}		–	33	–	nC
Gate Charge Total	Q_g	$V_{DD} = 480V, I_D = 20.7A, V_{GS} = 0 \text{ to } 10V$	–	87	114	nC
Gate Plateau Voltage	$V_{(plateau)}$	$V_{DD} = 480V, I_D = 20.7A$	–	5.5	–	V
Inverse Diode Continuous Forward Current	I_S	$T_C = 25^\circ\text{C}$	–	–	20.7	A
Inverse Diode Direct Current Pulsed	I_{SM}	$T_C = 25^\circ\text{C}$	–	–	62.1	A
Inverse Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_F = I_S$	–	1.0	1.2	V
Reverse Recovery Time	t_{rr}	$V_R = 480V, I_F = I_S, di_F/dt = 100A/\mu s$	–	500	800	ns
Reverse Recovery Charge	Q_{rr}		–	11	–	μC
Peak Reverse Recovery Current	I_{rrm}		–	70	–	A
Peak Rate of Fall of Reverse Recovery Current	di_{rr}/dt	$T_J = +25^\circ\text{C}$	–	1400	–	$A/\mu s$

Note 4. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Note 5. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

