NTE5470 thru 5476
Silicon Controlled Rectifier (SCR)
5 Amp, TO64

Description:
The NTE5470 through NTE5476 are multi-purpose PNPN silicon controlled rectifiers in a TO64 type stud mount package suitable for industrial and consumer applications.

Features:
- Uniform Low-Level Noise-Immune Gate Triggering
- Low Forward “ON” Voltage
- High Surge-Current Capability

Absolute Maximum Ratings: (Apply over operating temperature range unless otherwise specified)
- Peak Repetitive Forward and Reverse Blocking Voltage (Note 1), $V_{DRM}, V_{RRM}$
  - NTE5470: 50V
  - NTE5471: 100V
  - NTE5472: 200V
  - NTE5473: 300V
  - NTE5474: 400V
  - NTE5475: 500V
  - NTE5476: 600V
- Forward Current RMS, $I_{RMS}$: 8A
- Peak Forward Surge Current (One Cycle, 60Hz, $T_J = -40^\circ$ to $+100^\circ$C), $I_{TSM}$: 100A
- Circuit Fusing ($T_J = -40^\circ$ to $+100^\circ$C, $t \leq 8.3$ms), $I^2t$: 40A²sec
- Peak Gate Power, $P_{GM}$: 5W
- Average Gate Power, $P_{G(AV)}$: 0.5W
- Peak Gate Current, $I_{GM}$: 2A
- Peak Gate Voltage (Note 2), $V_{GM}$: 10V
- Operating Temperature Range, $T_J$: $-40^\circ$ to $+100^\circ$C
- Storage Temperature Range, $T_{stg}$: $-40^\circ$ to $+150^\circ$C
- Thermal Resistance, Junction-to-Case, $R_{thJC}$: 2.5°C/W
- Stud Torque: 15 in. lb.

Note 1. Ratings apply for zero or negative gate voltage. Devices should not be tested for blocking capability in a manner such that the voltage applied exceeds the rated blocking voltage.

Note 2. Devices should not be operated with a positive bias applied to the gate concurrently with a negative potential applied to the anode.
## Electrical Characteristics:  \((T_C = +25^\circ C\) unless otherwise specified)\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak Forward or Reverse Blocking Current</td>
<td>(I_{\text{DRM}}, I_{\text{RRM}})</td>
<td>Rated (V_{\text{DRM}}) or (V_{\text{RRM}}), Gate Open</td>
<td>(T_J = +25^\circ C)</td>
<td>–</td>
<td>–</td>
<td>10 (\mu A)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_J = +100^\circ C)</td>
<td>–</td>
<td>–</td>
<td>2</td>
<td>mA</td>
</tr>
<tr>
<td>Gate Trigger Current, Continuous DC</td>
<td>(I_{\text{GT}})</td>
<td>(V_D = 7V, R_L = 100\Omega, Note 3)</td>
<td>(T_C = -40^\circ C)</td>
<td>–</td>
<td>–</td>
<td>60 (mA)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(T_J = +100^\circ C)</td>
<td>–</td>
<td>10</td>
<td>30</td>
<td>mA</td>
</tr>
<tr>
<td>Gate Trigger Voltage, Continuous DC</td>
<td>(V_{\text{GT}})</td>
<td>(V_D = 7V, R_L = 100\Omega)</td>
<td>(T_C = -40^\circ C)</td>
<td>–</td>
<td>–</td>
<td>1.5</td>
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<tr>
<td></td>
<td></td>
<td>(T_J = +100^\circ C)</td>
<td>0.2</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Forward &quot;ON&quot; Voltage</td>
<td>(v_{\text{TM}})</td>
<td>(I_{\text{TM}} = 15.7A, Note 4)</td>
<td>(T_C = -40^\circ C)</td>
<td>–</td>
<td>1.4</td>
<td>2.0</td>
</tr>
<tr>
<td>Holding Current</td>
<td>(I_{\text{H}})</td>
<td>(V_D = 7V, Gate Open)</td>
<td>(T_C = -40^\circ C)</td>
<td>–</td>
<td>–</td>
<td>60</td>
</tr>
<tr>
<td>Turn–On Time ((t_d + t_r))</td>
<td>(t_{\text{on}})</td>
<td>(I_G = 20mA, I_F = 5A, V_D = \text{Rated } V_{\text{DRM}})</td>
<td>(T_J = +100^\circ C)</td>
<td>–</td>
<td>1</td>
<td>–</td>
</tr>
<tr>
<td>Turn–Off Time</td>
<td>(t_{\text{off}})</td>
<td>(I_F = 5A, I_R = 5A, V_D = \text{Rated } V_{\text{DRM}}, \frac{dv}{dt} = 30V/\mu s)</td>
<td>(T_J = +100^\circ C)</td>
<td>–</td>
<td>15</td>
<td>–</td>
</tr>
<tr>
<td>Forward Voltage Application Rate (Exponential)</td>
<td>(\frac{dv}{dt})</td>
<td>Gate Open, (T_J = +100^\circ C), (V_D = \text{Rated } V_{\text{DRM}})</td>
<td>(T_J = +100^\circ C)</td>
<td>–</td>
<td>25</td>
<td>–</td>
</tr>
</tbody>
</table>

**Note 3.** For optimum operation, i.e. faster turn–on, lower switching losses, best \(di/dt\) capability, recommended \(I_{\text{GT}} = 200mA\) minimum.

**Note 4.** Pulsed, 1ms Max, Duty Cycle \(\leq 1\%\).