

NTE7005 Integrated Circuit 2-Phase Stepping Motor Driver

Description:

The NTE7005 monolithic power IC is a dual bridge driver in a 16-Lead DIP type package. The maximum driving current and voltage is 330mA x 12V per bridge. Therefore, the best use for this part is in a two-phase bipolar stepping motor driving the head actuator of a 3, to 5.25-inch Floppy Disk Drive.

Features:

- 330mA Output Current Capability
- Dual Bridge Included
- Power Save
- Single Input Direction Control
- Low Output Saturation Voltage
- Low Supply Current
- Low Input Current
- Compatible with TTL, LSTTL, and 5V CMOS
- Thermal Shutdown

Absolute Maximum Ratings: ($T_A = +25^\circ\text{C}$, Note 1 unless otherwise specified)

| | |
|--|----------------|
| Logic Stage Supply Voltage, V_{CC} | 7V |
| Seeking Supply Voltage, V_{S1} | 15V |
| Holding Supply Voltage, V_{S2} | 7V |
| Input Voltage, V_i | 0 to V_{CC} |
| Peak Seeking Current ($t \leq 5\text{ms}$), $I_o(\text{peak})$ | 500mA |
| DC Seeking Current, I_{oS} | 330mA |
| DC Holding current, I_{OH} | 200mA |
| Power Dissipation (Note 2), P_T | 2W |
| Junction Temperature, T_J | +150°C |
| Operating Junction Temperature Range, T_{opr} | -20° to +125°C |
| Storage Temperature Range, T_{stg} | -55° to +125°C |

Note 1. The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Note 2. Thermal resistance is as follows:

- $R_{thJA1} \leq +60^\circ\text{C/W}$ (Soldered on a print circuit board)
- $R_{thJA2} \leq +35^\circ\text{C/W}$ (Soldered on a print circuit covered with copper sufficiently)
- $R_{thJA3} \leq +15^\circ\text{C/W}$ (Soldered on Pin4, Pin5, Pin12, and Pin13 with an infinite heat sink)

Recommended Operating Conditions:

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|----------------------------|----------|-----------------|------|------|------|------|
| Logic Stage Supply Voltage | V_{CC} | | 4.5 | 5.0 | 5.5 | V |
| Seeking Supply Voltage | V_{S1} | | 10.2 | 12.0 | 13.8 | V |
| Holding Supply Voltage | V_{S2} | | 4.5 | 5.0 | 5.5 | V |

Electrical Characteristics: ($T_A = +25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $V_{S2} = 5\text{V}$, $V_{S1} = 12\text{V}$ unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit | |
|-------------------------------------|----------------|--|-------------------|-----|----------|---------------|----|
| Input Low Voltage | V_{IL} | | – | – | 0.8 | V | |
| Input High Voltage | V_{IH} | | 2.0 | – | – | V | |
| Input Low Current | I_{IL} | $V_I = 0.8\text{V}$ | – | – | ± 10 | μA | |
| Input High Current | I_{IH} | $V_I = 2\text{V}$ | – | 1.0 | ± 10 | μA | |
| | | $V_I = 5.5\text{V}$ | – | 0.5 | 1.0 | mA | |
| Supply Current | I_{CC} | $PS = 0.8\text{V}$, $I_o = 0$ | V_{CC} | – | 25 | 33 | mA |
| | | | V_{S1} , Note 3 | – | 10 | 20 | mA |
| | | | V_{S2} , Note 4 | – | – | 1.0 | mA |
| | | $PS = 2\text{V}$, $I_o = 0$ | V_{CC} | – | 25 | 33 | mA |
| | | | V_{S1} , Note 3 | – | 3 | 5 | mA |
| | | | V_{S2} , Note 4 | – | 5 | 10 | mA |
| Output Transistor Breakdown Voltage | $V_{(BR)CE R}$ | $I_C = 10\text{mA}$ | 18 | – | – | V | |
| V_{S1} Saturation Voltage | $V_{CE(sat)1}$ | $PS = 0.8\text{V}$, $I_o = 330\text{mA}$, Note 5 | – | 1.5 | 2.0 | V | |
| V_{S2} Saturation Voltage | $V_{CE(sat)2}$ | $PS = 2\text{V}$, $I_o = 130\text{mA}$, Note 5 | – | 1.5 | 2.0 | V | |
| Clamp Diode Forward Voltage | V_F | $I_F = 330\text{mA}$ | Upper | – | 5 | – | V |
| | | | Lower | – | 1.5 | – | V |
| Delay Time | t_{PLH} | $I_o = 330\text{mA}$ | – | 1 | 5 | μs | |
| | t_{PHL} | | – | 1 | 5 | μs | |

Note 3. Sum of $V_{S1}(\phi 1)$ and $V_{S1}(\phi 2)$ current

Note 4. Sum of $V_{S2}(\phi 1)$ and $V_{S2}(\phi 2)$ current

Note 5. Sum of upper and lower saturation voltages

Truth Table (For each bridge):

| Power Save Direction | | ΦOut | $\bar{\Phi}\text{Out}$ |
|----------------------|---|------------------|------------------------|
| L | L | L | H+ |
| L | H | H+ | L |
| H | L | L | H– |
| H | H | H– | L |

Note: L = Low voltage state
 H+ = High voltage state
 (Seeking transistors ON)
 H– = High voltage state
 (Holding transistors ON)

Pin Connection Diagram

