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NTE7118
Integrated Circuit
Audio Power Amplifier, 50W

Description:

The NTE7118 integrated circuit is a hi–fi power amplifier in a 9–Lead SIP type package designed for use as a building block in radio, TV, and other audio applications. The high performance of the IC meets the requirements of digital sources (e.g. Compact Disc equipment).

The NTE7118 is totally protected, the two output transistors both having tthermal and SOAR protection. This device also has a mute function that can be arranged for a period after power–on with a delay time fixed by external components.

The NTE7118 device is intended for symmetrical power supplies but an asymmetrical supply may also be used.

Features:

- High Output Power (Also with Bootstrap)
- Low Offset Voltage
- Good Ripple Rejection
- Mute/Stand–by Facilities
- Thermal Protection
- Protected Against Electrostatic Discharge
- No Switch–On or Switch–Off Clicks
- Very Low Thermal Resistance
- Safe Operating Area (SOAR) Protection
- Short–Circuit Protection

Absolute Maximum Ratings:

Supply Voltage (Pin6 to Pin4), V_P . . . . . ±30V
Bootstrap Voltage (Pin7 to Pin4), V_{bstr} 70V
Output Current (Repetitive Peak), I_O 8A
Mute Voltage (Pin3 to Pin4), V_m 7V
Thermal Shut–Down Protection Time (Note 1), t_{pr} . . . . . 1 Hour
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Thermal Resistance, Junction–to–Mounting Base, $R_{th\ j–mb}$ 1K/W

Note 1. Symmetrical power supply: AC and DC short–circuit protected.
Asymmetrical power supply: AC short–circuit protected.
Driven by a pink–noise voltage.

Electrical Characteristics: (V_P = ±27.5V, R_L = 8Ω, f = 1kHz, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Range (Pin6 to Pin4)	V_P		±9	–	±30	V
Maximum Output Current (Peak Value)	I_{OMmax}		6.4	–	–	A
Operating State						
Input Voltage (Pin3 to Pin4)	$V_{3–4}$		6	–	7	V
Total Quiescent Current	I_{tot}	$R_L = \infty$	30	60	90	mA
Output Power	P_O	THD = –60dB	37	40	–	W
		THD = –20dB	–	51	–	W
		V_P = ±23V, THD = –60dB, R_L = 8Ω	–	28	–	W
		V_P = ±23V, THD = –60dB, R_L = 4Ω	–	50	–	W
Total Harmonic Distortion	THD	P_O = 32W	–	–90	–80	dB
Intermodulation Distortion	d_{im}	P_O = 32W, Note 2	–	–80	–	dB
Power Bandwidth	B	(–3dB) THD = –60dB	20 to 25,000			Hz
Slew Rate	dV/dt		–	10	–	V/µs
Closed Loop Voltage Gain	G_c	Note 3	–	30	–	dB
Open Loop Voltage Gain	G_o		–	85	–	dB
Input Impedance	$\|Z_i\|$	Note 4	1	–	–	MΩ
Signal–to–Noise Ratio	S/N	P_O = 50mW, Note 5	80	–	–	dB
Output Offset Voltage	V_O		–	2	*	V
Input Bias Current	I_I		–	0.1	*	µA
Output Impedance	$\|Z_o\|$		–	–	0.1	W
Supply Voltage Ripple Rejection	SVRR	Ripple Frequency = 100Hz, Ripply Voltage = 500mV_{eff}, (RMS Value) Source Resistance = 2kΩ	*	–	–	dB
Quiescent Current into Pin2	I_2	Note 6	–	–	*	µA
Mute State						
Voltage on Pin3	$V_{3–4}$		2	–	4.5	V
Offset Voltage	V_O		–	*	–	V
Output Voltage	V_O	$V_{i(rms)}$ = 2V, f = 1kHz	–	100	–	µV
Ripple Rejection	RR		–	70	–	dB
Standby State						
Voltage on Pin3	$V_{3–4}$		0	–	1	V
Total Quiescent Current	I_{tot}		–	20	–	mA
Ripple Rejection	RR		–	70	–	dB
Supply Voltage to Obtain Steady State	±V_P		4.5	–	7.0	V

* Value to be fixed.

Note 2. Measured with two superimposed signals of 50Hz and 7kHz with an amplitude relationship of 4:1.

Note 3. The closed loop gain is determined by external resistors and is variable between 20dB and 46dB.

Note 4. The input impedance is determined by the bias resistor.

Note 5. The noise output voltage is measured in a bandwidth of 20Hz to 20kHz with a source resistance of 2kΩ.

Note 6. The quiescent current into Pin2 has an impact on the mute time.

Pin Connection Diagram
(Front View)