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NTE7133 **Integrated Circuit** **Horizontal and Vertical Deflection Controller** **for VGA/XGA and Autosync Monitors**

Description:

The NTE7133 is an integrated circuit in a 20-Lead DIP type package. This device is designed to provide an economical solution in VGA/XGA and autosync monitors by incorporating complete horizontal and vertical small signal processing. VGA-dependent mode detection and setting are performed on-chip.

Features:

- VGA Operation Fully Implemented Including Alignment-Free Vertical and E/W Amplitude Pre-Settings
- 4th VGA Mode Easy Applicable (XGA, Super VGA)
- Autosync Operation Externally Selectable
- Low Jitter
- All Adjustments DC-Controllable
- Alignment-Free Oscillators
- Sync Separators for Video or Horizontal and Vertical TTL Sync Levels Regardless of Polarity
- Horizontal Oscillator with P_{LL1} for Sync and P_{LL2} for Flyback
- Constant Vertical and E/W Amplitude in Multi-Frequency Operation
- DC-Coupling to Vertical Power Amplifier
- Internal Supply Voltage Stabilization with Excellent Ripple Rejection to Ensure Stable Geometrical Adjustments

Absolute Maximum Ratings:

| | |
|--|----------------|
| Supply Voltage (Pin1), V _P | -0.5 to +16V |
| Voltage (Pin3, Pin7), V ₃ , V ₇ | -0.5 to +16V |
| Voltage (Pin8), V ₈ | -0.5 to +7V |
| Voltage (Pin5, Pin6, Pin9, Pin10, Pin13, Pin14, Pin18), V _n | -0.5 to +6.5V |
| Current (Pin2), I ₂ | ±10mA |
| Current (Pin3), I ₃ | 100mA |
| Current (Pin7), I ₇ | 20mA |
| Current (Pin8), I ₈ | -10mA |
| Electrostatic Handling for All Pins (Note 1), V _{esd} | ±400V |
| Operating Junction Temperature, T _J | +150°C |
| Operating Ambient Temperature Range, T _A | 0° to +70°C |
| Storage Temperature Range, T _{stg} | -55° to +150°C |
| Thermal Resistance, Junction-to-Ambient (In Free Air), R _{thJA} | 65K/W |

Note 1. Equivalent to discharging a 200pF capacitor through a 0Ω series resistor.

Electrical Characteristics: ($V_P = 12V$, $T_A = +25^\circ C$ unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---------------|--------------------------------------|-----|-------|----------|-------------|
| Supply | | | | | | |
| Positive Supply Voltage (Pin1) | V_P | | 9.2 | 12.0 | 16.0 | V |
| Supply Current | I_P | $I_{18} = -1.05mA$ | – | 36 | 44 | mA |
| | | $I_{18} = -3.388mA$ | – | 40 | 49 | mA |
| Internal Reference Voltage | | | | | | |
| Internal Reference Voltage | V_{ref} | | 6.0 | 6.25 | 6.5 | V |
| Temperature Coefficient | TC | $T_A = +20^\circ$ to $+100^\circ C$ | – | – | ± 90 | $10^{-6}/K$ |
| Power Supply Ripple Rejection | PSRR | f = 1kHz Sine Wave | 60 | 75 | – | dB |
| | | f = 1MHz Sine Wave | 25 | 35 | – | dB |
| Supply Voltage (Pin1) to Ensure All Internal Reference Voltages | V_P | | 9.2 | – | 16.0 | V |
| Composite Sync Input (AC–Coupled, $V_{10} = 5V$) | | | | | | |
| Sync Amplitude of Video Input Signal (Pin9) | $V_{i\ sync}$ | Sync on Green | – | 300 | – | mV |
| Top Sync Clamping Level | | | 1.1 | 1.28 | 1.5 | V |
| Slicing Level Above Top Sync Level | | Sync on Green, $R_S = 50\Omega$ | 90 | 120 | 150 | mV |
| Allowed Source Resistance for 7% Duty Cycle | R_S | $V_{i\ sync} > 200mV$ | – | – | 1.5 | k Ω |
| Differential Input Resistance | r_g | During Sync | – | 80 | – | Ω |
| Charging Current of Coupling Capacitor | I_g | $V_g > 1.5V$ | 1.3 | 2.0 | 3.0 | μA |
| Vertical Sync Integration Time to Generate Sync Pulse | t_{int} | $f_H = 31kHz$, $I_{18} = -1.050mA$ | 7 | 10 | 13 | μs |
| | | $f_H = 64kHz$, $I_{18} = -2.169mA$ | 3.5 | 5.0 | 6.5 | μs |
| | | $f_H = 100kHz$, $I_{18} = -3.388mA$ | 2.5 | 3.4 | 4.5 | μs |
| Horizontal Sync Input (DC–Coupled, TTL–Compatible) | | | | | | |
| Sync Input Signal (Peak Value, Pin9) | $V_{u\ sync}$ | | 1.7 | – | – | V |
| Slicing Level | | | 1.2 | 1.4 | 1.6 | V |
| Minimum Pulse Width | t_p | | 700 | – | – | ns |
| Rise Time and Fall Time | t_r , t_f | | 10 | – | 500 | ns |
| Input Current | I_g | $V_g = 0.8V$ | – | – | –200 | μA |
| | | $V_g = 5.5V$ | – | – | 10 | μA |
| Automatic Horizontal Polarity Switch (H–Sync on Pin9) | | | | | | |
| Horizontal Sync Pulse Width Related to t_H (Duty Cycle for Automatic Polarity Correction) | $t_p\ H/t_H$ | | – | – | 30 | % |
| Delay Time for Changing Sync Polarity | t_p | | 0.3 | – | 1.8 | ms |
| Vertical Sync Input (DC–Coupled, TTL–Compatible,,V–Sync on Pin10) | | | | | | |
| Sync Input Signal (Peak Value, Pin10) | $V_{i\ sync}$ | | 1.7 | – | – | V |
| Slicing Level | | | 1.2 | 1.4 | 1.6 | V |
| Input Current | I_{10} | $0 < V_{10} < 5.5V$ | – | – | ± 10 | μA |
| Maximum Vertical Sync Pulse Width for Automatic Vertical Polarity Switch | $t_p\ V$ | | – | – | 300 | μs |
| Horizontal Mode Detector Output (VGA Mode) | | | | | | |
| Output Saturation Voltage LOW (For Modes 1, 2, and 3) | V_7 | $I_7 = 6mA$ | – | 0.275 | 0.33 | V |
| Output Voltage HIGH | | Mode 4 | – | – | V_P | V |
| Load Current to Force VGA Mode–Dependent Vertical and Parabola Amplitudes | I_7 | Modes 1, 2, and 3 | 2 | – | 6 | mA |
| Output Current | | Mode 4 | – | 0 | – | mA |

Electrical Characteristics (Cont'd): ($V_P = 12V$, $T_A = +25^\circ C$ unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|------------------|---|--------------------|-------------------|-----------|-------------|
| VGA/Autosync Mode Switch | | | | | | |
| Input Voltage LOW to Force Autosync Mode | V_7 | | 0 | – | 50 | mV |
| Horizontal Comparator P_{LL1} | | | | | | |
| Upper Control Voltage Limitation | V_{17} | | – | 5.9 | – | V |
| Lower Control Voltage Limitation | | | – | 5.1 | – | V |
| Control Current | I_{17} | | – | $\pm 0.083I_{18}$ | – | μA |
| Horizontal Oscillator | | | | | | |
| Center Frequency | f_{OSC} | $R_{18} = 2.4k\Omega$ (Pin18), $C_{19} = 10nF$ (Pin19) | – | 31.45 | – | kHz |
| Deviation of Center Frequency | Δf_{OSC} | | – | – | ± 3.0 | % |
| Temperature Coefficient | TC | | – | +200 | +300 | $10^{-6}/K$ |
| Relative Holding/Catching Range | ϕ_H/t_H | | ± 6.0 | ± 6.5 | ± 7.3 | % |
| External Oscillator Current | I_{18} | | –0.5 | – | –4.3 | mA |
| Voltage at Reference Current Input (Pin18) | V_{18} | | 2.35 | 2.5 | 2.65 | V |
| Horizontal P_{LL2} | | | | | | |
| Upper Clamping Level of Flyback Input | V_2 | $I_2 = 6mA$ | – | 5.5 | – | V |
| Lower Clamping Level of Flyback Input | | $I_2 = -1mA$ | – | –0.75 | – | V |
| H–Flyback Slicing Level | | | – | 3.0 | – | V |
| Delay Between Middle of Sync and Middle of H–Flyback Related to t_H | t_d/t_H | | – | 3.0 | – | % |
| Upper Control Voltage Limitation | V_{20} | | – | 6.2 | – | V |
| Lower Control Voltage Limitation | | | – | 4.8 | – | V |
| Control Current | I_{20} | | – | $\pm 0.083I_{18}$ | – | μA |
| P _{LL2} Control range Related to t_H | $\Delta t/t_H$ | | 30 | – | – | % |
| Horizontal Output (Open–Collector) | | | | | | |
| Output Voltage LOW | V_3 | $I_3 = 20mA$ | – | – | 0.3 | V |
| | | $I_3 = 60mA$ | – | – | 0.8 | V |
| t_H Duty Cycle | t_p/t_H | | 42 | 45 | 48 | % |
| Threshold to Activate Too Low Supply Voltage Protection | V_P | Horizontal Output OFF | – | 5.6 | – | V |
| Threshold to Activate Too Low Supply Voltage Protection | | Horizontal Output ON | – | 5.8 | – | V |
| Jitter of Horizontal Output | Δt_H | $f = 31kHz$ | – | – | 3.5 | ns |
| | | $f = 64kHz$ | – | – | 1.9 | ns |
| | | $f = 100kHz$ | – | – | 1.2 | ns |
| Horizontal Clamping/Blanking Generator Output | | | | | | |
| Output Voltage LOW | V_8 | | – | – | 0.9 | V |
| Blanking Output Voltage | | Internal V Blanking | 1.6 | 1.9 | 2.2 | V |
| Clamping Output Voltage | | H–Sync on Pin9 | 5.15 | 5.4 | 5.65 | V |
| Internal Sink Current for All Output Levels | I_8 | H and V Scanning | 2.3 | 2.9 | 3.5 | mA |
| | | External Load Current | – | – | –3.0 | mA |
| Clamping Pulse Start | t_8 | | With End of H–Sync | | | |
| Clamping Pulse Width | t_{clp} | | 0.8 | 1.0 | 1.2 | μs |
| Steepness of Rise and Fall Times | S | | – | 60 | 75 | ns/V |

Electrical Characteristics (Cont'd): ($V_P = 12V$, $T_A = +25^\circ C$ unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|-----------------------|---|-------|-----------|-----------|-------------|
| Vertical Oscillator ($V_{ref} = 6.25V$) | | | | | | |
| Vertical Free-Running Frequency | f_o | $R_{15} = 22k\Omega$, $C_{16} = 0.1\mu F$ | – | 42 | – | Hz |
| Nominal Vertical Sync Range | f_V | No f_o Adjustment | 50 | – | 110 | Hz |
| Voltage on Pin15 | V_{15} | $R_{15} = 22k\Omega$ | 2.8 | 3.0 | 3.2 | V |
| Delay Between Sync Pulse and Start of Vertical Scan in VGA/XGA Mode | t_d | Measured on Pin8, Activated by an External Resistor on Pin7 | 500 | 575 | 650 | μs |
| Delay Between Sync Pulse and Start of Vertical Scan in Autosync Mode | | Measured on Pin8, $V_7 < 50mV$ | 240 | 300 | 360 | μs |
| Control Current for Amplitude Control | I_{12} | | – | ± 200 | – | μA |
| Capacitor for Amplitude Control | C_{12} | | – | – | 0.18 | μF |
| Vertical Differential Output | | | | | | |
| Differential Output Current Between Pin5 and Pin6 (Peak-to-Peak Value) | I_o | Mode 3, $I_{13} > -135\mu A$, $R_{15} = 22k\Omega$ | 0.9 | 1.0 | 1.1 | mA |
| Maximum Offset Current Error | | $I_o = 1mA$ | – | – | ± 2.5 | % |
| Maximum Linearity Error | | | – | – | ± 1.5 | % |
| Vertical Amplitude Adjustment (In Percent of Output Signal) | | | | | | |
| Input Voltage | V_{13} | | – | 5.0 | – | V |
| Adjustment Current | I_{13} | $I_{o\max}$ (100%) | –110 | –120 | –135 | μA |
| | | $I_{o\min}$ (Typically 58%) | – | 0 | – | μA |
| VGA Mode-Dependent Pre-Settings Activated by an External Resistor on Pin7 | $\Delta I_o/\Delta t$ | | | | | |
| Mode 1 | | Table 2, Note 2 | 116.1 | 116.8 | 117.4 | % |
| Mode 2 | | | 101.6 | 102.2 | 102.8 | % |
| Mode 3 | | | – | 100 | – | % |
| Mode 4 | | | – | 100 | – | % |
| Autosync Operation (VGA Operation Disabled) | | Table 2, Note 2, $V_7 < 50mV$ | – | 100 | – | % |
| E/W Output (Note 2) | | | | | | |
| Bottom Output Signal During Mid-Scan (Pin11) | V_{11} | Internally Stabilized | 1.05 | 1.2 | 1.35 | V |
| Top Output Signal During Flyback | | | 4.2 | 4.5 | 4.8 | V |
| Temperature Coefficient of Output Signal | TC | | – | – | 250 | $10^{-6}/K$ |
| E/W Amplitude Adjustment (Parabola) | | | | | | |
| Input Voltage (Pin14) | V_{14} | | – | 5.0 | – | V |
| Adjustment Current | I_{14} | 100% Parabola | –110 | –120 | –135 | μA |
| | | Typical 28% Parabola | – | 0 | – | μA |

Note 2. $\Delta I_o/\Delta t$ relative to value of Mode 3.

Note 3. Parabola amplitude tracks with mode-dependent vertical amplitude but not with vertical amplitude adjustment. Tracking can be achieved by a resistor from vertical amplitude potentiometer to Pin14.

Functional Description:

Horizontal Sync Separator and Polarity Correction

An AC-coupled video signal or a DC-coupled TTL sync signal (H only or composite sync) is input on Pin9. Video signals are clamped with top sync on 12.8V, and are sliced at 1.4V. This results in a fixed absolute slicing level of 120mV relative to top sync.

DC-coupled TTL sync signals are also sliced at 1.4V, however with the clamping circuit in current limitation. The polarity of the separated sync is detected by internal integration of the signal, then the polarity is corrected.

The polarity information is fed to the VGA mode detector. The corrected sync is the input signal for the vertical sync integrator and the P_{LL1} stage.

Vertical Sync Separator, Polarity Correction and Vertical Sync Integrator

DC-coupled vertical TTL sync signals may be applied to Pin10. They are sliced at 1.4V. The polarity of the separated sync is detected by internal integration, then polarity is corrected. The polarity information is fed to the VGA mode detector. If Pin10 is not used, it must be connected to GND.

The separated $V_{i\text{ sync}}$ signal from Pin10, or the integrated composite sync signal from Pin9 (TTL or video) directly triggers the vertical oscillator.

VGA Mode Detector and Mode Output

The three standard VGA modes and a 4th not fixed mode are decoded by the polarities of the horizontal and the vertical sync input signals. An external resistor (from V_P to Pin7) is necessary to match this function. In all three VGA modes the correct amplitudes are activated. The presence of the 4th mode is indicated by HIGH on Pin7. This signal can be used externally to switch any horizontal or vertical parameters.

VGA Mode Detector Input

For autosync operation the voltage on Pin7 must be externally forced to a level of < 50mV. Vertical amplitude pre-settings for VGA are then inhibited. The delay time between vertical trigger pulse and the start of vertical deflection changes from 575 to 300 μ s (575 μ s is needed for VGA). The vertical amplitude then remains constant in a frequency range from 50 to 110Hz.

Clamping and V-Blanking Generator

A combined clamping and V-blanking pulse is available on Pin8. The lower level of 1.9V is the blanking signal derived from the vertical blanking pulse from the internal vertical oscillator.

Vertical blanking equals the delay between vertical sync and the start of vertical scan. By this, an optimum blanking is achieved for VGA/XGA as well as for multi-frequency operation (selectable via Pin7).

The upper level of 5.4V is the horizontal clamping pulse with internally fixed pulse width of 0.8 μ s. A mono flop, which is triggered by the trailing edge of the horizontal sync pulse, generates this pulse. If composite sync is applied one clamping pulse per H-period is generated during V-sync. The pulse of the clamping pulse may change during V-sync.

P_{LL1} Phase Detector

The phase detector is a standard one using switched current sources. The middle of the sync is compared with a fixed point of the oscillator sawtooth voltage. The PLL filter is connected to Pin17. If composite sync is applied, the distributed control voltage is corrected during V-sync.

Horizontal Oscillator

This oscillator is a relaxation type and requires a fixed capacitor of 10nF at Pin19. By changing the current into Pin18 the whole frequency range from 13 to 100kHz can be covered.

The current can be generated either by a frequency to voltage converter or by a resistor. A frequency adjustment may also be added if necessary.

The P_{LL1} control voltage at Pin17 modulates via a buffer stage the oscillator thresholds. A high DC-loop gain ensures a stable phase relationship between horizontal sync and line flyback pulses.

Functional Description (Cont'd):

P_{LL2} Phase Detector

This phase detector is similar to the P_{LL1} phase detector. Line flyback signals (Pin2) are compared with a fixed point of the oscillator sawtooth voltage. Delays in the horizontal deflection circuit are compensated by adjusting the phase relationship between horizontal sync and horizontal output pulses.

A certain amount of phase adjustment is possible by injecting a DC current from an external source into the P_{LL2} filter capacitor on Pin20.

Horizontal Driver

This open-collector output stage (Pin3) can directly drive an external driver transistor. The saturation voltage is 300mV at 20mA. To protect the line deflection transistor, the horizontal output stage does not conduct at $V_P < 6.4V$ (Pin1).

Vertical Oscillator and Amplitude Control

This stage is designed for fast stabilization of the vertical amplitude after changes in sync conditions.

The free-running frequency f_o is determined by the values of R_{VOS} and C_{VOS} . The recommended values should be altered marginally only to preserve the excellent linearity and noise performance. The vertical drive currents I_5 and I_6 are in relation to the value of R_{VOS} . Therefore, the oscillator frequency must be determined only by C_{VOS} on Pin16.

$$f_o = \frac{1}{10.8 \times R_{VOS} \times C_{VOS}}$$

To achieve a stabilized amplitude the free-running frequency f_o (without adjustment) must be lower than the lowest occurring sync frequency. The contributions shown in Table 1 can be assumed.

Table 1. Calculation of f_o Total Spread

| Contributing Elements | % |
|---|-----------|
| Minimum Frequency Offset Between f_o and the Lowest Trigger Frequency | 10 |
| Spread of IC | ±3 |
| Spread of R (22kΩ) | ±1 |
| Spread of C (0.1μF) | ±5 |
| Total | 19 |

Results for 50 to 110Hz application: $f_o = \frac{50\text{Hz}}{1.19} = 42\text{Hz}$

Table 2. VGA Modes

| Mode | Horizontal/Vertical Sync Polarity | Horizontal Frequency (kHz) | Vertical Frequency (Hz) | Number of Active Lines | Output Mode Pin7 |
|-------------|--|-----------------------------------|--------------------------------|-------------------------------|-------------------------|
| 1 | +/- | 31.45 | 70 | 350 | LOW |
| 2 | -/+ | 31.45 | 70 | 400 | LOW |
| 3 | -/- | 31.45 | 60 | 480 | LOW |
| 4 | +/+ | Fixed by External Circuitry | — | — | HIGH |
| Autosync | */* | Fixed by External Circuitry | — | — | Forced to GND |

Pin Connection Diagram

| | | | |
|----------------------------------|-----------|-----------|---------------------------------------|
| V_P | 1 | 20 | P _{LL2} Phase |
| Horiz Flyback Input | 2 | 19 | Horiz OSC Capacitor |
| Horiz Output | 3 | 18 | Horiz OSC Resistor |
| GND (0V) | 4 | 17 | P _{LL1} Phase |
| Vert Output 1/Neg-Going Sawtooth | 5 | 16 | Vert OSC Capacitor |
| Vert Output 2/Pos-Going Sawtooth | 6 | 15 | Vert OSC Resistor |
| 4th Mode Output/Autosync In | 7 | 14 | E/W Amp Adj Input (Parabola) |
| Clamping/Blanking Pulse Out | 8 | 13 | Vert Amp Adj Input |
| Horiz Sync/Video In | 9 | 12 | Cap for Amp Control |
| Vert Sync In | 10 | 11 | E/W Output (Parabola to Driver Stage) |

