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NTE7134
Integrated Circuit
Horizontal and Vertical Deflection Controller for Monitors

Description:

The NTE7134 is a high performance and efficient solution for autosync monitors in a 32–Lead DIP type package. The concept is fully DC controllable and can be used in applications with a microcontroller and stand–alone in rock bottom solutions.

This device provides synchronization processing, H + V synchronization with full autosync capability, and very short setting times after mode changes. External power components are givena great deal of protection. The IC generates the drive waveforms for DC–coupled vertical boosters.

The NTE7134 provides ectended functions e.g. as a flexible SMPS block and an extensive set of geometry control facilities, providing excellent picture quality.

Features:

Concept Features

- Full Horizontal (H) Plus Vertical (V) Autosync Capability
- Completely DC Controllable for Analog and Digital Concepts
- Excellent Geometry Control Functions (e.g. Automatic Correction of East–West (EW) Parabola During Adjustment of Vertical Size and Vertical Shift)
- Felxible Switched Mode Power Supply (SMPS) Function Block for Feedback and Feed Forward Converters.
- X–Ray Protection
- Start–Up and Switch–Off Sequences for safe Operation of All Power Components
- Very Good Vertical Linearity
- Internal Supply Voltage Stabilization

Synchronization Inputs

- Can Handle All Sync Signals (Horizontal, Vertical, Composite and Sync–On–Video)
- Combined Output for Video Clamping, Vertical Blanking and Protection Blanking
- Start of Video Clamping Pulses Externally Selectable

Horizontal Section

- Extremely Low Jitter
- Frequency Locked Loop for Smooth Catching of Line Frequrncy
- Simple Frequency Preset of f_{min} and f_{max} by External Resistors
- DC Controllable Wdie Range Linear Picture Position
- Soft Start for Horizontal Driver

Vertical Section

- Vertical Amplitude Independent of Frequency
- DC Controllable Picture Height, Picture Position and S–Correction
- Differential Current Outputs for DC Coupling to Vertical Booster

Features (Cont'd):

EW Section

- Output for DC Adjustable EW Parabola
- DC Controllable Picture Width and Trapezium Correction
- Optional Tracking of EW Parabola with Line Frequency
- Prepared for Additional DC Controls of Vertical Linearity, EW–Corner, EW Pin Balance, EW Parallelogram, Vertical Focus by Extended Application

Absolute Maximum Ratings: (All voltages measured with respect to GND)

Supply Voltage (Pin9), V_{CC} . . . . . –0.5 to +16V

Input Voltages, $V_{I(n)}$

- Pin5 . . . . . –0.5 to +6.0V
- Pin15, Pin17, Pin18, Pin19, Pin23, Pin28, Pin30 . . . . . –0.5 to +6.5V
- Pin2 . . . . . –0.5 to +8.0V
- Pin10 . . . . . –0.5 to +16V

Output Voltages, $V_{O(n)}$

- Pin12, Pin13 . . . . . –0.5 to +6.5V
- Pin6, Pin7 . . . . . –0.5 to +16V

Input/Output Voltages, $V_{IO(n)}$

- Pin3, Pin4 . . . . . –0.5 to +6.0V
- Pin14 . . . . . –0.5 to +6.5V

Horizontal Driver Output Current, I_{HDRV} . . . . . –10 to +10mA

Horizontal Flyback Input Current, I_{HFLB} 100mA

Video Clamping Pulse/Vertical Blanking Output Current, I_{CLBL} . . . . . –10mA

B+ Control OTA Output Current, I_{BOP} 1mA

B+ Control Driver Output Current, I_{BDRV} 50mA

EW Driver Output Current, I_{EWDRV} . . . . . –5mA

Electrostatic Discharge for All Pins (Note 1), V_{esd}

- Machine Model . . . . . ±400V
- Human Body Model . . . . . ±3000V

Operating Junction Temperature, T_J . . . . . +150°C

Operating Ambient Temperatrure Range, T_A . . . . . 0° to +70°C

Storage Temperature Range, T_{stg} . . . . . –55° to +150°C

Thermal Resistance, Junction–to–Ambient (In Free Air), R_{thJA} 55K/W

Note 1. Machine model: 200pF, 25Ω, 2.5µH; Human body model: 100pF, 1500Ω, 7.5µH.

Electrical Characteristics: (V_P = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Horizontal Sync Separator						
Input Characteristics for DC–Coupled TTL Signals [HSYNC (Pin15)]						
Sync Input Signal Voltage	$V_{DC(HSYNC)}$		1.7	–	–	V
Slicing Voltage Level			1.2	1.4	1.6	V
Rise Time of Sync Pulse	$t_{r(HSYNC)}$		10	–	500	ns
Fall Time of Sync Pulse	$t_{f(HSYNC)}$		10	–	500	ns
Minimum Width of Sync Pulse	$t_{W(HSYNC)}$		0.7	–	–	µs
Input Current	$I_{DC(HSYNC)}$	V_{HSYNC} = 0.8V	–	–	–200	µA
		V_{HSYNC} = 5.5V				µA

Electrical Characteristics (Cont'd): (V_P = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Horizontal Sync Separator (Cont'd)						
Input Characteristics for AC–Coupled Video Signals (Sync–on–Video, Negative Sync Polarity)						
Sync Amplitude of Video Input Signal Voltage	$V_{AC(HSYNC)}$		–	300	–	mV
Slicing Voltage Level (Measured from Top Sync)		R_S = 50Ω	90	120	150	mV
Top Sync Clamping Level	$V_{clamp(HSYNC)}$		1.1	1.28	1.5	V
Charge Current for Coupling Capacitor	$I_{C(HSYNC)}$	$V_{HSYNC} > V_{clamp(HSYNC)}$	1.7	2.4	3.4	µA
Minimum Width of Sync Pulse	$t_{HSYNC(min)}$		0.7	–	–	µs
Maximum Source Resistance	$R_{S(max)}$	Duty factor = 7%	–	–	1500	Ω
Differential Input Resistance	$r_{diff(HSYNC)}$	During Sync	–	80	–	Ω
Automatic Polarity Correction for Horizontal Sync						
Horizontal Sync Pulse Width Related to t_H	$\frac{t_{p(H)}}{t_H}$	f_H < 45kHz	–	–	20	%
		f_H > 45kHz	–	–	25	&
Delay Time for Changing Polarity	$t_{p(H)}$		0.3	–	1.8	ms
Vertical Sync Integrator						
Integration Time for Generation of a Vertical Trigger Pulse	$t_{int(V)}$	f_H = 31.45kHz, I_{HREF} = 1.052mA	7.0	10.0	13.0	µs
		f_H = 64kHz, I_{HREF} = 2.141mA	3.9	5.7	6.5	µs
		f_H = 100kHz, I_{HREF} = 3.345mA	2.5	3.8	4.5	µs
Vertical Sync Slicer (DC–Coupled, TTL Compatible) [VSYNC (Pin14)]						
Sync Input Signal Voltage	V_{VSYNC}		1.7	–	–	V
Slicing Voltage Level			1.2	1.4	1.6	V
Input Current	I_{VSYNC}	0V < V_{SYNC} < 5.5V	–	–	±10	µA
Vertical Sync Output at VSYNC (Pin14) During Composite Sync at HSYNC (Pin15)						
Output Current	I_{VSYNC}	During Internal Vertical Sync	–0.7	–1.0	–1.35	mA
Internal Clamping Voltage Level	V_{VSYNC}	During Internal Vertical Sync	4.4	4.8	5.2	V
Steepness of Slopes			–	300	–	ns/mA
Automatic Polarity Correction for Vertical Sync						
Maximum Width of Vertical Sync Pulse	$t_{VSYNC(max)}$		–	–	300	µs
Delay for Change Polarity	$t_{d(VPOL)}$		0.3	–	1.8	ms
Video Clamping/Vertical Blanking Output [CLCB (Pin16)]						
Width of Video Clamping Pulse	$t_{clamp(CLBL)}$	Measured at V_{CLBL} = 3V	0.6	0.7	0.8	µs
Temperature Coefficient of $V_{clamp(CLCB)}$	TC_{clamp}		–	+4	–	mV/K
Steepness of Slopes for Clamping Pulse		R_L = 1MΩ, C_L = 20pF	–	50	–	ns/V
Top Voltage Level of Vertical Blanking Pulse	$V_{blank(CLBL)}$	Note 2	1.7	1.9	2.1	V
Width of Vertical Blanking Pulse	$t_{blank(CLBL)}$		240	300	360	µs

Note 2. Continuous blanking at CLCB (Pin16) will be activated, if one of the following conditions is true:

a) No horizontal flyback pulse at HFLB (Pin1) within a line
b) X–ray protection is triggered
c) Voltage at HPLL2 (Pin31) is low (for soft start of horizontal drive)
d) Supply voltage at V_{VV} (Pin9) is low
e) PLL1 unlocked while frequency–locked loop is in search mode

Electrical Characteristics (Cont'd): (V_P = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Video Clamping/Vertical Blanking Output (Cont'd) [CLCB (Pin16)]						
Temperature Coefficient of $V_{blank(CLBL)}$	TC_{blank}		–	+2	–	mV/K
Output Voltage During Vertical Scan	$V_{scan(CLBL)}$	I_{CLBL} = 0	0.59	0.63	0.67	V
Temperature Coefficient of $V_{scan(CLBL)}$	TC_{scan}		–	–2	–	mV/K
Internal Sink Current	$I_{sink(CLBL)}$		2.4	–	–	mA
External Load Current	$I_{load(CLBL)}$		–	–	–3.0	mA
Selection of Leading/Trailing Edge for Video Clamping Pulse						
Voltage at CLSEL (Pin10) for Trigger with Leading Edge of Horizontal Sync	V_{CLSEL}		7	–	V_{CC}	V
Voltage at CLSEL (Pin10) for Trigger with Trailing Edge of Horizontal Sync			0	–	5	V
Delay Between Leading Edge of Horizontal Sync and Start of Horizontal Clamping Pulse	$t_{d(clamp)}$	V_{CLSEL} > 7V	–	300	–	ns
Delay Between Leading Trailing of Horizontal Sync and Start of Horizontal Clamping Pulse		V_{CLSEL} < 5V	–	130	–	ns
Maximum Duration of Video Clamping Pulse After End of Horizontal Sync	$t_{clamp(max)}$	V_{CLBL} = 3V, V_{CLSEL} > 7V	–	–	0.15	µs
		V_{CLBL} = 3V, V_{CLSEL} > 5V	–	–	1.0	µs
Input Resistance at CLSEL (Pin10)	R_{CLSEL}	$V_{CLSEL} \le V_{CC}$	80	–	–	kΩ
PLL1 Phase Comparator and Frequency–Locked Loop [HPLL1 (Pin26) and HBUF (Pin27)]						
Maximum Width of Horizontal Sync Pulse (Referenced to Line Period)	$t_{HSYNC(max)}$	f_H < 45kHz, Note 2	–	–	20	&
		f_H > 45kHz, Note 3	–	–	25	%
Total Lock–In Time of PLL1	$t_{lock(HPLL1)}$		–	40	80	ms
Control Voltage	V_{HPLL1}	Note 4, Note 5				
Buffered f/v Voltage at HBUF (Pin27)	V_{HBUF}	$f_{H(min)}$, Note 6	–	5.6	–	V
		$f_{H(max)}$, Note 6	–	2.5	–	V
Maximum Load Current	$I_{load(HBUF)}$		–	–	–4.0	mA
Adjustment of Horizontal Picture Position						
Horizontal Shift Adjustment Range (Referenced to Horizontal Period)	ΔHPOS	I_{HSHIFT} = 0	–	–10.5	–	%
		I_{HSHIFT} = –135µA	–	+10.5	–	%
Input Current	I_{HPOS}	ΔHPOS = +10.5%	–110	–120	–135	µA
		ΔHPOS = –10.5%	–	0	–	µA

Note 3. To ensure safe locking of the horizontal oscillator, one of the following procedures is required:
a) Search mode starts always from f_{min}. Then the PLL1 filter components are a 3.3nF capacitor from Pin26 to GND in parallel with an 8.2kΩ resistor in series with a 47nF capacitor.
b) Search mode starts either from f_{min} or f_{max} with HPOS in middle position (I_{HPOS} = 60µA). Then the PLL1 filter components are a 1.5nF capacitor from Pin26 to GND in parallel with a 27kΩ resistor in series with a 47nF capacitor.
c) After locking is achieved, HPOS can be operated in the normal way

Note 4. Loading of HPLL1 (Pin26) is not allowed.

Note 5. Oscillator frequency is f_{min} when no sync signal is present (no continuous blanking at Pin16).

Note 6. Voltage at HPPL1 (Pin26) is fed to HBUF (Pin27) via a buffer. Disturbances caused by horizontal sync are removed by an internal sample–and–hold circuit.

Electrical Characteristics (Cont'd): (V_P = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Adjustment of Horizontal Picture Position (Cont'd)						
Reference Voltage at Input	$V_{ref(HPOS)}$	Note 7	–	5.1	–	V
Picture Shift is Centered if HPOS (Pin30) is Forced to GND	$V_{off(HPOS)}$		0	–	0.1	V
Horizontal Oscillator [HCAP (Pin29) and HREF (Pin28)]						
Free–Running Frequency Without PLL1 Action (For Testing Only)	$f_{H(0)}$	$R_{HBUF} = \infty$, R_{HREF} = 2.4kΩ, C_{HCAP} = 10nF, Note 5	30.53	31.45	32.39	kHz
Spread of Free–Running Frequency (Excluding Spread of External Components)	$\Delta f_{H(0)}$		–	–	±3.0	%
Temperature Coefficient of Free–Running Frequency	TC		–100	–	+100	10^{-6}/K
Maximum Oscillator Frequency	$f_{H(max)}$		–	–	130	kHz
Voltage at Input for Reference Current	V_{HREF}		2.43	2.55	2.68	V
PLL2 Phase Detector [HFLB (Pin1) and HPPL2 (Pin31)]						
PLL2 Control (Advance of Horizontal Drive with Respect to Middle of Horizontal Flyback)	$\Delta\phi_{PLL2}$	Maximum Advance	36	–	–	%
		Minimum Advance	–	7	–	%
Delay Between Middle of Horizontal Sync and Middle of Horizontal Flyback	$t_{d(HFLB)}$	HPOS (Pin30) Grounded	–	200	–	ns
Maximum Voltage for PLL2 Protection Mode/Soft Start	$V_{PROT(HPLL2)}$		–	4.4	–	V
Charge Current for External Capacitor During Soft Start	$I_{charge(HPLL2)}$	V_{HPLL2} < 3.7V	–	15	–	µA
Horizontal Flyback Input [HFLB (Pin1)]						
Positive Clamping Level	V_{HFLB}	I_{HFLB} = 5mA	–	5.5	–	V
Negative Clamping Level		I_{HFLB} = –1mA	–	–0.75	–	V
Positive Clamping Current	I_{HFLB}		–	–	6	mA
Negative Clamping Current			–	–	–2	mA
Slicing Level	V_{HFLB}		–	2.8	–	V
Output Stage for Line Driver Pulses [HDRV (Pin7)]						
Open Collector Output Stage						
Saturation Voltage	V_{HDRV}	I_{HDRV} = 20mA	–	–	0.3	V
		I_{HDRV} = 60mA	–	–	0.8	V
Output Leakage Current	$I_{leakage(HDRV)}$	V_{HDRV} = 16V	–	–	10	µA
Automatic Variation of Duty Factor						
Relative t_{OFF} Time of HDRV Output Measured at V_{HDRV} = 3V, HDRV Duty Factor is Determined by the Relation I_{HREF}/I_{VREF}	$t_{HDRV(OFF)}/t_H$	I_{HDRV} = 20mA, f_H = 31.45kHz	42.0	45.0	48.0	%
		I_{HDRV} = 20mA, f_H = 57kHz	45.0	46.3	47.7	%
		I_{HDRV} = 20mA, f_H = 90kHz	46.6	48.0	49.4	%

Note 5. Oscillator frequency is f_{min} when no sync signal is present (no continuous blanking at Pin16).

Note 7. Input resistance at HPOS (Pin30): $R_{HPOS} = \frac{kT}{q} \times \frac{1}{I_{HPOS}}$

Electrical Characteristics (Cont'd): (V_P = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
X–Ray Protection [XRAY (Pin2)]						
Slicing Voltage Level	V_{XRAY}		6.14	6.38	6.64	V
Minimum Width of Trigger Pulse	$t_{W(XRAY)}$		10	–		µs
Input Resistance at XRAY (Pin2)	$R_{I(XRAY)}$	$V_{XRAY} < 6.38V + V_{BE}$	500	–	–	kΩ
		$V_{XRAY} > 6.38V + V_{BE}$	–	5	–	kΩ
Supply Voltage for Reset of X–Ray Latch	$V_{RESET(VCC)}$		–	5.6	–	V
Vertical Oscillator (Oscillator Frequency in Application Without Adjustment of Free–Running Frequency $f_{V(o)}$)						
Free–Running Frequency	f_V	R_{VREF} = 22kΩ, C_{VCAP} = 100nF	40.0	42.0	43.3	Hz
Vertical Frequency Catching Range	$f_{V(o)}$	Constant Amplitude, Note 8, Note 9, Note 10	50	–	110	Hz
Voltage at Reference Input for Vertical Oscillator	V_{VREF}		–	3.0	–	V
Delay Between Trigger Pulsed and Start of Ramp at VCAP (Pin24) (Width of Vertical Blanking Pulse)	$t_{d(scan)}$		240	300	360	µs
Control Currents of Amplitude Control	I_{VAGC}		±120	±200	±300	µA
External Capacitor at VAGC (Pin22)	C_{VAGC}		–	–	150	nF
Differential Vertical Current Outputs						
Adjustment of Vertical Size [VAMP (Pin18)]						
Vertical Size Adjustment Range (Referenced to Nominal Vertical Size)	ΔVAMP	I_{VAMP} = 0, Note 11	–	60	–	%
		I_{VAMP} = –135µA, Note 11	–	100	–	%
Input Current for Max Amplitude (100%)	I_{VAMP}		–110	–120	–135	µA
Input Current for Min Amplitude (60%)			–	0	–	µA
Reference Voltage at Input	$V_{ref(VAMP)}$		–	5.0	–	V
Adjustment of Vertical Shift [VPOS (Pin17)]						
Vertical Shift Adjustment Range (Referenced to 100% Vertical Size)	ΔVPOS	I_{VPOS} = –135µA, Note 11	–	–11.5	–	%
		I_{VPOS} = 0, Note 11	–	+11.5	–	%
Input Current for Max Shift–Up	I_{VPOS}		–110	–120	–135	µA
Input Current for Max Shift–Down			–	0	–	µA
Reference Voltage at Input	$V_{ref(VPOS)}$		–	5.0	–	V
Vertical Shift is Centered of VPOS (Pin17) is Forced to GND	$V_{off(VPOS)}$		0	–	0.1	V

Note 8. Full vertical sync range with constant amplitude ($f_{V(min)}$: $f_{V(max)}$ = 1 : 2.5) can be made by chosing an application with adjustment of free–running frequency.

Note 9. If higher vertical frequencies are reqiured, sync range can be shifted by using a smaller capacitor at VCAP (Pin24).

Note 10. Value of resistor at VREF (Pin23) may not be changed.

Note 11. All vertical and EW adjustments are specified at nominal vertical settings, which means:

a) ΔVAMP = 100% (I_{VAMP} = 135µA

b) ΔVSCOR = 0 (Pin19 Open–Circuit)

c) ΔVPOS centered (Pin17 forced to GND)

d) f_H = 70kHz

Electrical Characteristics (Cont'd): (V_P = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Vertical Current Outputs (Cont'd)						
Adjustment of Vertical S–Correction [VSCOR (Pin19)]						
Vertical S–Correction Adjustment Range	ΔVSCOR	I_{VSCOR} = 0, Note 11	–	2	–	%
		I_{VSCOR} = –135μA, Note 11	–	46	–	%
Input Current for Max S–Correction	I_{VSCOR}		–110	–120	–135	μA
Input Current for Min S–Correction			–	0	–	μA
Symmetry Error of S–Correction	δVSCOR	Maximum ΔVSCOR	–	–	±0.7	%
Reference Voltage at Input	$V_{ref(VSCOR)}$		–	5.0	–	V
Voltage Amplitude of Superimposed Logarithmic Sawtooth (Peak–to–Peak Value)	$V_{SAWM(p–p)}$	Note 12	–	–	145	mV
Vertical Output Stage [VOUT1 (Pin13) and VOUT2 (Pin12)]						
Nominal Differential Output Current (Peak–to–Peak Value) ($\lvert\Delta I_{VOUT}\rvert = I_{VOUT1} – I_{VOUT2}$)	$\Delta I_{VOUT(nom)}$	Nominal Settings, Note 11	0.76	0.85	0.94	mA
Maximum Differential Output Current (Peak Value) ($\lvert\Delta I_{VOUT}\rvert = I_{VOUT1} – I_{VOUT2}$)	$\Delta I_{VOUT(max)}$		0.47	0.52	0.57	mA
Allowed Voltage at Outputs	V_{VOUT1}, V_{VOUT2}		0	–	4.2	V
Maximum Offset Error of Vertical Output Currents	$\delta_{V(offset)}$	Nominal Settings, Note 11	–	–	±2.5	%
Maximum Linearity Error of Vertical Output Currents	$\delta_{V(lin)}$	Nominal Settings, Note 11			±1.5	%
EW Drive Output						
EW Drive Output Stage [EWDRV (Pin11)]						
Bottom Output Voltage (Internally Stabilized)	V_{EWDRV}	$V_{PAR(EWDRV)}$ = 0, $V_{DC(EWDRV)}$ = 0, EWTRP Centered	1.05	1.20	1.35	V
Maximum Output Voltage		Note 13	7.0	–	–	V
Output Load Current	I_{EWDRV}		–	–	±2.0	mA
Temperature Coefficient of Output Signal	TC_{EWDRV}		–	–	600	$10^{–6}$/K
Adjustment of EW Parabola Amplitude [EWPAR (Pin21)]						
Parabola Amplitude	$V_{PAR(EWDRV)}$	I_{EWPAR} = 0, Note 11	–	0.05	–	V
		I_{EWPAR} = –135μA, Note 11	–	3	–	V

Note 11. All vertical and EW adjustments are specified at nominal vertical settings, which means:
- a) ΔVAMP = 100% (I_{VAMP} = 135μA
- b) ΔVSCOR = 0 (Pin19 Open–Circuit)
- c) ΔVPOS centered (Pin17 forced to GND)
- d) f_H = 70kHz

Note 12. The superimposed logarithmic sawtooth at VSCOR (Pin19) tracks with VPOS, but **not** with VAMP settings.

The superimposed waveform is described by $\frac{kT}{q} \times \ln\frac{1–d}{1+d}$ with 'd' being the modulation depth of a sawtooth from $–^5/_6$ to $+^5/_6$. A linear sawtooth with the same modulation depth can be recovered in an external long–tail pair.

Note 13. The output signal at EWDRV (Pin11) may consist of parabola + DC shift + trapezium correction. These adjustments have to be carried out in a correct relationship to each other to avoid clipping due to the limited output voltage range at EWDRV.

Electrical Characteristics (Cont'd): (V_P = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EW Drive Output (Cont'd)						
Adjustment of EW Parabola Amplitude (Cont'd) [EWPAR (Pin21)]						
Input Current for Maximum Amplitude	I_{EWPAR}		–110	–120	–135	µA
Input Current for Minimum Amplitude			–	0	–	µA
Reference Voltage at Input	$V_{ref(EWPAR)}$		–	5.0	–	V
Adjustment of Horizontal Size [EWWID (Pin32)]						
EW Parabola DC Voltage Shift	$V_{DC(EWDRV)}$	I_{EWWID} = –135µA, Note 11	–	0.1	–	V
		I_{EWWID} = 0, Note 11	–	4.2	–	V
Input Current for Maximum DC Shift	I_{EWWID}		–	0	–	µA
Input Current for Minimum DC Shift			–110	–120	–135	µA
Reference Voltage at Input	$V_{ref(EWWID)}$		–	5.0	–	V
Adjustment of Trapezium Correction [EWTRP (Pin20)]						
Trapezium Correction Voltage	$V_{TRP(EWTRP)}$	I_{EWTRP} = 0, Note 11	–	–0.5	–	V
		I_{EWTRP} = –135µA, Note 11	–	+0.5	–	V
Input Current for Maximum Positive Trapezium Correction	I_{EWTRP}		–110	–120	–135	µA
Input Current for Maximum Negative Trapezium Correction			–	0	–	µA
Reference Voltage at Input	$V_{ref(EWTRP)}$		–	5.0	–	V
Trapezium Correction is Centered if EWTRP (Pin20) is Forced to GND	$V_{off(EWTRP)}$		0	–	0.1	V
Amplitude of Superimposed Logarithmic Parabola (Peak–to–Peak Value)	$V_{PARM(p-p)}$	Note 14	–	–	145	mV
Tracking of EWDRV Output Signal with f_H Proportional Voltage						
f_H Range for Tracking	$f_{H(MULTI)}$		24	–	80	kHz
Parabola Amplitude at EWDRV (Pin11)	$V_{PAR(EWDRV)}$	I_{HREF} = 1.052mA, F_H = 31.45kHz, Note 15	1.30	1.45	1.60	V
		I_{HREF} = 2.341mA, F_H = 70kHz, Note 15	2.7	3.0	3.3	V
		Function Disabled, Note 15	2.7	3.0	3.3	V
Linearity Error of f_H Tracking	δV_{EWDRV}		–	–	8	%
Voltage Range to Inhibit Tracking	V_{EWWID}		0	–	0.1	V
B+ Control Section						
Transconductance Amplifier [BIN (Pin5) and BOP (Pin3)]						
Input Voltage	V_{BIN}		0	–	5.25	V
Maximum Input Current	$I_{BIN(max)}$		–	–	±1	µA

Note 11. All vertical and EW adjustments are specified at nominal vertical settings, which means:
- a) ΔVAMP = 100% (I_{VAMP} = 135µA
- b) ΔVSCOR = 0 (Pin19 Open–Circuit)
- c) ΔVPOS centered (Pin17 forced to GND)
- d) f_H = 70kHz

Note 14. The superimposed logarithmic parabola at EWTRP (Pin20) tracks with VPOS, but **not** with VAMP settings.

Note 15. If f_H tracking is enabled, the amplitude of the complete EWDRV output signal (parabola + DC shift + trapezium) will be changed proportional to I_{HREF}. The EWDRV low level of 1.2V remains fixed.

Electrical Characteristics (Cont'd): (V_P = 12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
B+ Control Section (Cont'd)						
Transconductance Amplifier (Cont'd) [BIN (Pin5) and BOP (Pin3)]						
Reference Voltage at Internal Non–Inverting Input of OTA	$V_{ref(int)}$		2.37	2.50	2.58	V
Minimum Output Voltage	$V_{BOP(min)}$		–	0.4	–	V
Maximum Output Voltage	$V_{BOP(max)}$	I_{BOP} < 1mA	5.0	5.3	5.6	V
Maximum Output Current	$I_{BOP(max)}$		–	±500	–	μA
Transconductance of OTA	g	Note 16	30	50	70	mS
Open–Loop Gain	G_{open}		–	86	–	dB
Minimum Value of Capacitor at BOP (Pin3)	C_{BOP}		4.7	–	–	nF
Voltage Comparator [BSENS (Pin4)]						
Voltage Range of Positive Comparator Input	V_{BSENS}		0	–	5	V
Voltage Range of Negative Comparator Input	V_{BOP}		0	–	5	V
Maximum Leakage Current	I_{BSENS}	Discharge Disabled	–	–	–2	μA
Open Collector Output Stage [BDRV (Pin6)]						
Maximum Output Current	$I_{BDRV(max)}$		20	–	–	mA
Output Leakage Current	$I_{leakage(BDRV)}$	V_{BDRV} = 16V	–	–	3	μA
Saturation Voltage	$V_{sat(BDRV)}$	I_{BDRV} < 20mA	–	–	300	mV
Minimum Off–Time	$t_{off(min)}$		–	250	–	ns
Delay Between BDRV Pulse and HDRV Pulse (Rising Edges)	$t_{d(BDRV)}$	Measured at V_{HDRV}, V_{BDRV} = 3V	–	500	–	ns
BSENS Discharge Circuit						
Discharge Stop Level	$V_{STOP(BSENS)}$	Capacitive Load, I_{BSENS} = 0.5mA	0.85	1.0	1.15	V
Discharge Current	$I_{DISC(BSENS)}$	V_{BSENS} > 2.5V	4.5	6.0	7.5	mA
Threshold Voltage for Restart	$V_{RESTART(BSENS)}$	Fault Condition	1.2	1.3	1.4	V
Minimum Value of Capacitor at BSENS (Pin4)	C_{BSENS}		2	–	–	nF
Internal Reference, Supply Voltage and Protection						
External Supply Voltage for Complete Stabilization of All Internal References	$V_{STAB(VCC)}$		9.2	–	16	V
Supply Current	I_{VCC}		–	49	–	mA
Power Supply Rejection Ratio of Internal Supply Voltage	PSRR	f = 1kHz	50	–	–	dB

Note 16. First pole of the transconductance amplifier is 5MHz without an external capacitor (will become the second pole, if the OTA operates as an integrator).

Functional Description:

Horizontal Sync Separator and Polarity Correction

HSYNC (Pin15) is the input for horizontal synchronization signals, which can be DC–coupled TTL signals (horizontal or composite sync) and AC–coupled negative–going video sync signals. Video syncs are clamped to 1.28V and sliced at 1.4V. This results in a fixed absolute slicing level of 120mV related to sync top.

For DC–coupled TTL signals the input clamping current is limited. The slicing level for TTL signals is 1.4V.

The separated sync signal (either video or TTL) is integrated on an internal capacitor to detect and normalize the sync polarity.

Normalized horizontal sync pulses are used as input signals for the vertical sync integrator, the PLL1 phase detector and the frequency–locked loop.

Vertical Sync Integrator

Normalized composite sync signals from HSYNC are integrated on an internal capacitor in order to extract vertical sync pulses. The integration time is dependent on the horizontal oscillator reference current at HREF (Pin28). The integrator output directly triggers the vertical oscillator. This signal is available at VSYNC (normally vertical sync input; Pin14), which is used as an output in this mode.

Vertical Sync Slicer and Polarity Correction

Vertical sync signals (TTL) applied to VSYNC (Pin14) are sliced at 1.4V. The output signal of the sync slicer is integrated on an internal capacitor to detect and normalize the sync polarity.

If a composite sync signal is detected at HSYNC, VSYNC is used as output for the integrated vertical sync (e.g. for power saving applications).

Video Clamping/Vertical Blanking Generator

The video clamping/vertical blanking signal at CLBL (Pin16) is a two–level sandcastle pulse which is especially suitable for video ICs, but also for direct applications in video output stages.

The upper level is the video clamping pulse, which is triggered by the trailing edge of the horizontal sync pulse. The width of the video clamping pulse is determined by an internal monoflop.

CLSEL (Pin10) is the selection input for the position of the video clamping pulse. If CLSEL is connected to GND, the clamping pulse is triggered with the trailing edge of horizontal sync. For a clamping pulse which starts with the leading edge of horizontal sync, Pin10 must be connected to V_{CC}.

The lower level of the sandcastle pulse is the vertical blanking pulse, which is derived directly from the internal oscillator waveform. It is started by the vertical sync and stopped with the start of the vertical scan. This results in optimum vertical blanking.

Blanking will be activated continuously, if one of the following conditions is true:

No horizontal flyback pulses at HFLB (Pin1)
X–ray protection is activated
Soft start of horizontal drive (voltage at HPPL2 (Pin31) is low)
Supply voltage at V_{CC} (Pin9) is low
PLL1 is unlocked while frequency–locked loop is in search mode

Blanking will not be activated if the horizontal sync frequency is below the valid range or there are no sync pulses available.

Functional Description (Cont'd):

Frequency–Locked Loop

The frequency–locked loop can lock the horizontal oscillator over a wide frequency range. This is achieved by a combined search and PLL operation. The frequency range is preset by two external resistors and the recommended ratio is $\frac{f_{min}}{f_{max}} = \frac{1}{3.5}$

Larger ranges are possible by extended applications.

Without a horizontal sync signal the oscillator will be free–running at f_{min}. Any change of sync conditions is detected by the internal coincidence detector. A deviation of more than 4% between horizontal sync and oscillator frequency switches the horizontal section into search mode. This means that PLL1 control currents are switched off immediately. Then the internal frequency detector starts tuning the oscillator. Very small DC currents at HPLL1 (Pin26) are used to perform this tuning with a well defined change rate. When coincidence between horizontal sync and oscillator frequency is detected, the search mode is replaced by a normal PLL operation. This operation ensures a smooth tuning and avoids fast changes of horizontal frequency during catching.

In this concept it is not allowed to load HPLL1. The frequency dependent voltage at this pin is fed internally to HBUF (Pin27) via a sample–and–hold and buffer stage. The sample–and–hold stage removes all disturbances caused by horizontal sync or composite vertical sync from the buffered voltage. An external resistor from HBUF to HREF defines the frequency range.

See also hints for locking procedure in Note 2 of the "Electrical Characteristics" section of this data sheet.

P_{LL1} Phase Detector

The phase detector is a standard type using switched current sources. The middle of the horizontal sync is compared with a fixed point of the oscillator sawtooth voltage. The PLL1 loop filter is connected to HPLL (Pin26).

Horizontal Oscillator

This oscillator is a relaxation type and requires a fixed capacitor of 10nF at HCAP (Pin29). For optimum jitter performance the value of 10nF must not be changed.

The maximum oscillator frequency is determined by a resistor from HREF to GND. A resistor from HREF to HBUF defines the frequency range.

The reference current at HREF also defines the integration time constant of the vertical sync integration.

Calculation of Line Frequency Range

First the oscillator frequencies f_{min} and f_{max} have to be calculated. This is achieved by adding the spread of the relevant components to the highest and lowest sync frequencies $f_{S(min)}$ and $f_{S(max)}$. The oscillator is driven by the difference of the currents in R_{HREF} and R_{HBUF}. At the highest oscillator frequency R_{HBUF} does not contribute to the spread. The spread will increase towards lower frequencies due to the contribution of R_{HBUF}. It is also dependent on the ratio $\frac{f_{S(max)}}{f_{S(min)}}$

The following example is a 31.45 to 64kHz application: $n_s = \frac{f_{S(max)}}{f_{S(min)}} = \frac{64kHz}{31.45kHz} = 2.04$

Table 1. Calculation of total spread

spread of:	for f_{max}	for f_{min}
IC	3%	3%
C_{HCAP}	2%	2%
R_{HREF}	1%	–
R_{HREF}, R_{HBUF}	–	1% x (2.3 x n_s –1)
Total	6%	8,69%

Functional Description (Cont'd):

Calculation of Line Frequency Range (Cont'd)

Thus the typical frequency range of the oscillator in this example is:

$f_{max} = f_{S(max)} \times 1.06 = 67.84kHz$

$f_{min} = \frac{f_{S(min)}}{1.087} = 28.93kHz$

The resistors R_{HREF} and R_{HBUF} can be calculated with the following formula:

$R_{HREF} = \frac{74 \times kHz \times k\Omega}{f_{max}\,[kHz]} = 1.091k\Omega$

$R_{HBUF} = \frac{R_{HREF} \times 1.19 \times n}{n - 1} = 1.091k\Omega$

Where: $n = \frac{f_{max}}{f_{min}} = 2.35$

The spread of f_{min} increases with the frequency ratio $\frac{f_{S(max)}}{f_{S(min)}}$

For higher ratios this spread can be reduced by using resistors with less tolerances.

P_{LL2} Phase Detector

The PLL2 phase detector is similiar to the PLL1 detecrtor and compares the line flyback pulse at HFLB (Pin1) with the oscillator sawtooth voltage. The PLL2 detector thus compensates for the delay in the external horizontal deflection circuit by adjusting the phase of the HDRV (Pin7) output pulse.

The phase between horizontal flyback and horizontal sync can be controlled at HPOS (Pin30).

If HPLL2 is pulled to GND, horizontal output pulses, vertical output currents and B+ control pulses are inhibited. This means, HDRV (Pin7), BDRV (Pin6) VOUT1 (Pin13) and VOUT2 (Pin12) are floating in this state. PLL2 and the frequency–locked loop are disabled, and CLCB (Pin16) provides a continuous blanking signal.

This option can be used for soft start, protection and power–down modes. When the HPLL2 voltage is released again, an automatic soft start sequence will be performed.

The soft start timing is determined by the filter capacitor at HPLL2 (Pin31), which is charged with a constant current during soft start. In the beginning the horizontal driver stage generates very small output pulses. The width of thses pulses increases with the voltage at HPLL2 until the final duty factor is reached. At this point BDRV (Pin6), VOUT1 (Pin13 and VOUT2 (Pin12) are re–enabled. The voltage at HPLL2 continues to rise until PLL2 enters its normal operating range. The internal charge current is now disabled. Finally PLL2 and the frequency–locked loop are enabled, and the continuous blanking at CLBL is removed.

Horizontal Phase Adjustment

HPOS (Pin30) provides a linear adjustment of the relative phase between the horizontal sync and oscillator sawtooth. Once adjusted, the relative pahse remains constant over the whole frequency range.

Application hint: HPOS is a current input, which provides an internal reference voltage while I_{HPOS} is in the specified adjustment current range, By grounding HPOS the symmetrical control range is forced to its center value, therefore the pahse between horizontal sync and horizontal drive pulse is only determined by PLL2.

Output Stage for Line Drive Pulses

An open collector output stage allows direct drive of an inverting driver transistor because of a low saturation voltage of 0.3V at 20mA. To protect the line deflection transistor, the output stage is disabled (floating) for low supply voltage at V_{CC}.

The duty factor of line drive pulses is slightly dependent on the actual line frequency. This ensures optimum drive conditions over the whole frequency range.

Functional Description (Cont'd):

X–Ray Protection

The X–ray protection input XRAY (Pin2) provides a voltage detector with a precise threshold. If the input voltage at XRAY exceeds this threshold for a certain time, an internal latch switches the IC into protection mode. In this mode several pins are forced into defined states:

Horizontal output stage (HDRV) is floating
B+ control driver stage (BDRV) is floating
Vertical output stages (VOUT1 and VOUT2) are floating
CLBL provides a continuous blanking signal
The capacitor connected to HPLL2 (Pin31) is discharged

To reset the latch and return to normal operation, V_{CC} has to be temporaily switched off.

Vertical Oscillator and Amplitude Control

This stage is designed for fast stabilization of vertical amplitude after changes in sync frequency conditions. The free–running frequency $f_{osc(V)}$ is determined by the resistor R_{VREF} connected to Pin23 and the capacitor C_{VCAP} connected to Pin24. The value of R_{VREF} is not only optimized for noise and linearity performance in the whole vertical and EW section, but also influences several internal references, Therefore the value of R_{VREF} must not be changed. capacitor C_{VCAP} should be used to select the free–running frequency of the vertical oscillator in accordance with the following formula:

$$fosc(V) = \frac{1}{10.8 \times R_{VREF} \times C_{VCAP}}$$

To achieve a stabilized amplitude the free–running frequency $f_{osc(V)}$, without adjustment, should be at least 10% lower than the minimum trigger frequency. The contributions shown in Table 2 can be assumed.

Table 2. Calculation of $f_{osc(V)}$ total spreads

Contributing elements:	
Minimum frequency offset between $f_{osc(V)}$ and lowest trigger frequency	±10%
Spread of IC	±3%
Spread of R_{VREF}	±1%
Spread of C_{VCAP}	±5%
Total	19%

Results for 50 to 110Hz application: $f_{osc(V)} = \frac{50Hz}{1.19} = 42Hz$

Application hint: VAGC (Pin22) has a high input impedance during scan, thus the pin must not be loaded externally. Otherwise non–linearities in the vertical output currents may occur due to the changing charge current during scan.

Application hint: The full vertical sync range of 1 : 2.5 can be made usable by incorporating an adjustment of the free–running frequency. Also the complete sync range can be shifted to higher frequencies (e.g. 70 to 160Hz) by reducing the value of C_{VCAP}.

Adjustment of Vertical Size, Vertical Shift and S–Correction

VPOS (Pin17) is the input for the DC adjustable vertical picture shift. This pin provides a phase shift at the sawttoth output VOUT1 and VOUT2 (Pin13 and Pin12) and the EW drive output EWDRV (Pin11) in such a way that the whole picture moves vertically while maintaining the correct geometry.

The amplitude of the differential output currents at VOUT1 and VOUT2 can be adjusted via input VAMP (Pin18). This can be a combination of a DC adjustment and a dynamic waveform modulation.

VSCOR (pin19) is used to adjust the amount of vertical S–correction in the output signal.

Functional Description (Cont'd):

Adjustment of Vertical Size, Vertical Shift and S–Correction (Cont'd)

The adjustments for vertical size and vertical shift also affect the wavweforms of the EW parabola and the vertical S–correction. The result of this interaction is that no readjustment of these parameters is necessary after an adjustment of vertical picture size or position.

Application hint: VPOS is a current input which provides an internal reference voltage while I_{VPOS} is in the specified adjustment current range. By grounding VPOS (Pin17) the symmetrical control range is forced to its center value.

Application hint: VSCOR is a current input at 5V. Superimposed on this level is a very small positive–going vertical sawtooth, intended to modulate an external long–tailed transistor pair. This enables further optional DC controls of functions which are not directly accessible such as vertical tilt or vertical linearity.

EW Parabola (Including Horizontal Size and Trapezium Correction)

EWDRV (Pin11) provides a complete EW drive waveform. EW parabola amplitude, DC shift (horizontal size) and trapezium correction can be controlled via separate DC inputs.

EWPAR (Pin21) is used to adjust the parabola amplitude. This can be a combination of a DC adjustment and a dynamic waveform modulation.

The EW parabola amplitude also tracks with vertical picture size. The parabola waveform itself tracks with the adjustment for vertical picture shift (VPOS).

EWWID (Pin32) offers two modes of operation:

Mode 1 Horizontal size is DC controlled via EWWID (Pin32) and causes a DC shift at the EWDRV output. Also the complete waveform is multiplied internally by a signal proportional to the line frequency (which is detected via the current at HREF (Pin28). This mode is to be used for driving EW modulator stages which require a voltage proportional to the line frequency.

Mode 2 EWWID (Pin32) is grounded. Then EWDRV is no longer multiplied by the line frequency. The DC adjustment for horizontal size must be added to the input of the B+ control amplifier BIN (Pin5). This mode is to be used for driving EW modulations which require a voltage independent of the line frequency.

EWTRP (Pin20 is used to adjust the amount of trapezium correction in the EW drive waveform.

Application hint: EWTRP (Pin20) is a current input at 5V. Superimposed on this level is a very small vertical parabola with positive tips, intended to modulate an external long–tailed transistor pair. This enables further optional DC controls of functions which are not directly accessible such as EW–corner, vertical focus or EW pin balance.

Application hint: By grounding EWTRP (Pin20) the symmetrical control range is forced to its center value.

B+ Control Function Block

The B+ control function block of the EASDC consists of an Operatgional Transcondutance Amplifier (OTA), a voltage comparator, a flip–flop and a discharge circuit. This configuration allows easy applications for different B+ control concepts.

General Description

The non–inverting input of the OTA is connected internally to a high precision reference voltage. The inverting input is connected to BIN (Pin5). An internal clamping circuit limits the maximum positive output voltage of the OTA. The output itself is connected to BOP (Pin3) and to the inverting inpuyt of the voltage comparator. The non–inverting input of the voltage comparator can be accessed via BSENS (Pin4).

Functional Description (Cont'd):

B+ Control Function Block (Cont'd)

B+ drive pulses are generated by an internal flip–flop and fed to BDRV (Pin6) vai an open collector output stage. This flip–flop will be set at the rising edge of the signal at HDRV (Pin7). The falling edge of the output signal at BDRV has a defined delay of $t_{d(BDRV)}$ to the rising edge of the HDRV pulse. When the voltage at BSENS exceeds the voltage at BOP, the voltage comparator output resets the flip–flop and therefore, the open collector stage at BDRV is floating again.

An internal discharge circuit allows a well defined discharge of capacitors at BSENS. BDRV is active at a low level output voltage thus, it requires an external inverting driver stage.

The B+ function block can be used for B+ deflection modulators in either of two modes:

- Feedback Mode
  In this application the OTA is used as an error amplifier with a limited output voltage range. The flip–flop will be set at the rising edge of the signal at HDRV. A reset will be generated when the voltage at BSENS taken from the current sense resistor exceeds the voltage at BOP.

  If not reset is generated within a line period, the rising edge of the next HDRV pulse forces the flip–flop to reset. The flip–flop is set immediately after the voltage at BSENS has been dropped below the threshold voltage $V_{RESTART(BSENS)}$.
- Feed Forward Mode
  This application uses an external RC combination at BSENS to provide a pulse width which is independent from the horizontal frequency. The capacitor is charged via an external resistor and discharged by the internal discharge circuit. For normal operation the discharge circuit is activated when the flip–flop is reset by the internal voltage comparator. Now the capacitor will be discharged with a constant current until the internally controlled stop level $V_{STOP(BSENS)}$ is reached. This level will be maintained until the rising edge of the next HDRV pulse sets the flip–flop again and disables the discharge circuit.

  If no reset is generated within a line period, the rising edge of the next HDRV pulse automatically starts the discharge sequence and resets the flip–flop. When the voltage at BSENS reaches the threshold voltage $V_{RESTART(BSENS)}$, the discharge circuit will be disabled automatically and the flip–flop will be set immediately. This behaviour allows a definition of the maximum duty cycle of the B+ control drive pulse by the relationship of charge current to discharge current.

Supply Voltage Stabilizer, Reference and Protection

The ASDC provides an internal supply voltage stabilizer for excellent stabilization of all internal references. An internal gap reference especially designed for low–noise is the reference for the internal horizontal and vertical supply voltages. All internal reference currents and drive current for the vertical output stage are derived from this voltage via external resistors.

A special protection mode has been implemented in order to protect the deflection stages and the picture tube during start–up, shut–down and fault conditions. This protection mode can be activated as shown in Table 3.

Table 3. Activation of protection mode

Activation	Reset
Low Supply Voltage at Pin9	Increase Supply Voltage
X–Ray Protection XRAY (Pin2) Triggered	Remove Supply Voltage
HPLL2 (Pin31) Pulled to GND	Release Pin31

Functional Description (Cont'd):

Supply Voltage Stabilizer, Reference and Protection (Cont'd)

When protection mode is active, several pins of the ASDC are forced into a defined state:

HDRV (Horizontal Driver Output) is floating
BDRV (B+ Control Driver Output) is floating
VOUT1 and VOUT2 (Vertical Outputs) are floating
CLBL provides a continuous blanking signal
The capacitor at HPLL2 is discharged

If the protection mode is activated via the supply voltage at Pin9, all thesae actions will be performed in a well defined sequence. For activation via X–ray protection or HPLL2 all actions will occur simultaneously.

The return to normal operation is performed in accordance with the start–up sequence, if the reset was caused by the supply voltage at Pin9. The first action with increasing supply voltage is the activation of continuous blanking at CLBL. When the threshold for activation of HDRV is passed, an internal current begins to sharge the external capacitor at HPLL2 and PLL2 soft start sequence is performed. In the beginning of this phase the horizontal driver stage generates very small output pulses. The width of these pulses increases with the voltage at HPLL2 until the final duty cycle is reached. Then the PLL2 voltage passes the threshold for activation of BDRV, VOUT1 and VOUT2.

For activation of these pins not only the PLL2 voltage, but also the supply voltage, must have passed the appropriate threshold. A last pair of thresholds has to be passed by PLL2 voltage **and** supply voltage before the continuous blanking is finally removed, and the operation of PLL2 and frequency–locked loop is enabled.

A return to the normal operation by releasing the voltage at HPLL2 will lead to a slightly different sequence. Here the activation of all functions is influenced only by the voltage at HPPL2.

Application hint: Internal discharge of the capacitor at HPLL2 will only be performed, if the protection mode was activated via the supply voltage or X–ray protection.

Pin Connection Diagram