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NTE7147 Integrated Circuit Full Bridge Current Driven Vertical Deflection Booster

Description:

The NTE7147 is a power amplifier in a 9-Lead SIP type package designed for use in 90 degree color vertical deflection systems for frame frequencies of 50Hz to 160Hz. This device provides a high CMRR current driven differential input. Due to the bridge configuration of the two output stages, DC-coupling of the deflection coil is achieved.

Features:

- Pre-Amplifier with Differential High CMRR Current Mode Inputs
- Low Offsets
- High Linear Sawtooth Signal Amplification
- High Efficient DC-Coupled Vertical Output Bridge Circuit
- Powerless Vertical Shift
- High Deflection Frequency up to 160Hz
- Power Supply and Flyback Supply Voltage Independent Adjustable to Optimize Power Consumption and Flyback Time
- Excellent Transition Behaviour During Flyback
- Guard Circuit for Screen Protection

Absolute Maximum Ratings: (Voltage referenced to Pin5 (GND) unless otherwise specified)

Supply Voltage (Pin3), V _P	30V
Flyback Supply Voltage (Pin7), V _{FB}	60V
Flyback Supply Current, I _{FB}	±1.8A
Input Voltage, V ₁ , V ₂	0 to V _P V
Input Current, I ₁ , I ₂	0 to ±5mA
Output Voltage, V ₄ , V ₆	0 to V _P V
Output Current (Note 1), I ₄ , I ₆	0 to ±1.8A
Feedback Voltage, V ₉	0 to V _P V
Feedback Current, I ₉	0 to ±5mA
Guard Voltage (Note 2), V ₈	0 to V _P +0.4V
Guard Current, I ₈	0 to ±5mA
Operating Junction Temperature Range (Note 3), T _J	-20° to +150°C
Ambient Temperature Range, T _A	-20° to +75°C
Storage Temperature Range, T _{stg}	-20° to +150°C
Thermal Resistance, Junction-to-Mounting Base, R _{thJ-MB}	4K/W
Electrostatic Handling Voltage (Note 4), V _{es}	-500V to +500V

Note 1. Maximum output currents I₄ and I₆ are limited by current protection.

Note 2. For V_P > 13V, the guard voltage V₈ is limited to 13V.

Note 3. Internally limited by thermal protection; switching point ≥ +150°C.

Note 4. Equivalent to discharging a 200pF capacitor through a 0Ω series resistor,

Electrical Characteristics: ($V_P = 15V$, $T_A = +25^\circ C$, $V_{FB} = 40V$, voltage referenced to Pin5 (GND) unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (Pin3)	V_P		8.2	—	25	V
Flyback Supply Voltage (Pin7)	V_{FB}	Note 5	V_P+6	—	60	V
Quiescent Feedback Current (Pin7)	I_{FB}	No Load, No Signal	—	7	10	mA
Input Stage						
Differential Input Current ($I_{id} = I_1 - I_2$) (Peak-to-Peak Value)	$I_{id(p-p)}$		—	± 500	± 600	μA
Single Ended Input Current (Peak-to-Peak Value)	$I_{1,2(p-p)}$	Note 6	0	± 300	± 600	μA
Common Mode Rejection Ratio	CMRR	Note 7	—	-54	—	dB
Input Clamp Voltage	V_1	$I_1 = 300\mu A$	2.7	3.0	3.3	V
	V_2	$I_2 = 300\mu A$	2.7	3.0	3.3	V
Input Clamp Signal TC on Pin1	$TC_{i,1}$		0	—	± 800	$\mu V/K$
Input Clamp Signal TC on Pin2	$TC_{i,2}$		0	—	± 800	$\mu V/K$
Differential Input Voltage	$V_1 - V_2$	$I_{id} = 0$	0	—	± 10	mV
Feedback Current	I_9		—	± 500	± 600	μA
Feedback Voltage	V_9		1	—	V_P-1	V
Differential Input Offset Current ($I_{id(offset)} = I_1 - I_2$)	$I_{id(offset)}$	$I_{defl} = 0, R_{ref} = 1.5k\Omega, R_m = 1\Omega$	0	—	± 20	μA
Input Capacity Pin1 Reference to GND	$C_{i INA}$		—	—	5	pF
Input Capacity Pin2 Reference to GND	$C_{i INB}$		—	—	5	pF
Output Stages A and B						
Output Current	I_4, I_6		—	—	± 1	A
Output A Saturation Voltage to GND	V_6	$I_6 = 0.7A$	—	1.3	1.5	V
		$I_6 = 1.0A$	—	1.6	1.8	V
Output A Saturation Voltage to V_P	$V_{6,3}$	$I_6 = 0.7A$	—	2.3	2.9	V
		$I_6 = 1.0A$	—	2.7	3.3	V
Output B Saturation Voltage to GND	V_4	$I_4 = 0.7A$	—	1.3	1.5	V
		$I_4 = 1.0A$	—	1.6	1.8	V
Output B Saturation Voltage to V_P	$V_{4,3}$	$I_4 = 0.7A$	—	1.0	1.6	V
		$I_4 = 1.0A$	—	1.3	1.9	V
Linearity Error	LE	$I_{defl} = \pm 0.7A$, Note 8	—	—	2	%

Note 5. Up to $60V \geq V_{FB} \geq 40V$ a decoupling capacitor $C_{FB} = 22\mu F$ (between Pin7 and Pin5) and a resistor $R_{FB} = 100\Omega$ (between Pin7 and V_{FB}) are required.

Note 6. Saturation voltages of output stages A and B can be increased in the event of negative input currents $I_{1,2} < -500\mu A$.

Note 7. $D_i = \frac{I_{deflc}}{I_{idc}} \times \frac{I_{id}}{I_{defl}}$ with I_{deflc} = common mode deflection current and I_{idc} = common mode input current.

Note 8. Deviation of the output slope at a constant input slope.

Electrical Characteristics (Cont'd): ($V_P = 15V$, $T_A = +25^\circ C$, $V_{FB} = 40V$, voltage referenced to Pin5 (GND) unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Stages A and B (Cont'd)						
DC Output Voltage	V_4, V_6	$I_{id} = 0A$, Closed-Loop	6.6	7.2	7.8	V
Open-Loop Current Gain ($I_{4,6}/I_{id}$)	G_{oi}	$I_{4,6} < 100mA$, Note 9	-	100	-	dB
Open-Loop Current Gain ($I_{4,6}/I_9$)	G_{ofb}	$I_{4,6} < 100mA$, Note 9	-	100	-	dB
Current Ratio (I_{id}/I_9)	G_{ifb}	Closed-Loop	-	-0.2	-	dB
Output Ripple Current as a Function of Supply Ripple	$I_{defl(ripple)}$	$V_{P(ripple)} = \pm 0.5V$, $I_{id} = 0$, Closed-Loop	-	± 1	-	mA
Flyback Generator						
Voltage Drop During Flyback Reverse	$V_{7,6}$	$I_{defl} = 0.7A$	-	-2.0	-3.0	V
		$defl = 1.0A$	-	-2.3	-3.5	V
		$defl = 0.7A$	-	+5.6	+6.1	V
		$defl = 1.0A$	-	+5.9	+6.5	V
Switching On Threshold Voltage	V_6		$V_P - 1$	-	$V_P + 1.5$	V
Switching Off Threshold Voltage	V_6		$V_P - 1.5$	-	$V_P + 1$	V
Flyback Current During Flyback	I_7		-	-	± 1	A
Guard Circuit						
Output Voltage	V_8	Guard On	7.5	8.5	10	V
		Guard On, $V_P = 8.2V$	6.9	-	$V_P - 0.4$	V
		Guard Off	-	-	0.4	V
Output Current	I_8	Guard On	5	-	-	mA
		Guard Off, $V_8 = 5V$	0.5	1.0	1.5	mA
Allowable External Voltage on Pin8	$V_{8(ext.)}$		0	-	13	V
		$V_P \leq 13V$	0	-	$V_P + 0.3$	V

Note 9. Frequency behaviour of G_{oi} and G_{ofb} .

- a) -3dB open-loop bandwidth (-45°) at 15kHz; second pole (-135°) at 1.3MHz.
- b) Open-loop gain at second pole (-135°) 55dB.

Pin Connection Diagram

(Front View)



9 Feedback Input

8 Guard Output

7 Flyback Supply Voltage

6 Output A

5 GND

4 Output B

3 V_P

2 Input B

1 Input A

