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## **NTE7161** **Integrated Circuit** **Horizontal & Vertical Deflection** **for Autosync Monitors**

### **Description:**

The NTE7161 is a monolithic integrated circuit in a 20-Lead DIP type package designed for economical solutions in autosync monitors. This device incorporates the complete horizontal and vertical small signal processing on a single chip. When used in conjunction with the NTE7135 or NTE7156 vertical output circuits, this device offers an extremely advanced system solution.

### **Features:**

- Low Jitter
- All Adjustments DC-Controllable
- Alignment-Free Oscillators
- Sync Separators for Video or Horizontal and Vertical TTL Sync Levels Regardless of Polarity
- Horizontal Oscillator with PLL1 for Sync and PLL2 for Flyback
- Constant Vertical and E/W Amplitude in Autosync Operation
- DC-Coupling to Vertical Power Amplifier
- Internal Supply Voltage Stabilization with Excellent Ripple Rejection to Ensure Stable Geometrical Adjustments

### **Absolute Maximum Ratings:**

Supply Voltage (Pin1), $V_P$	–0.5 to 16V
Voltage on Pin3, $V_3$	–0.5 to 16V
Voltage on Pin8, $V_8$	–0.5 to 7V
Voltage on Pin5, Pin6, Pin9, Pin10, Pin13, Pin14 and Pin18, $V_n$	–0.5 to 6.5V
Current on Pin2, $I_2$	$\pm 10\text{mA}$
Current on Pin3, $I_3$	100mA
Current on Pin8, $I_8$	–10mA
Maximum Junction Temperature, $T_J$	+150°C
Operating Ambient Temperature Range, $T_A$	0° to +70°C
Storage Temperature Range, $T_{stg}$	–55° to +150°C
Thermal Resistance, Junction-to-Ambient (In free air), $R_{thJA}$	65K/W
Electrostatic Handling (For All Pins, Note 1), $V_{ESD}$	$\pm 400\text{V}$

Note 1. Equivalent to discharging a 200pF capacitor through a 0Ω series resistor.

**Electrical Characteristics:** ( $V_P = 12V$ ,  $T_A = +25^\circ C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Positive Supply Voltage (Pin1)	V <sub>P</sub>		9.2	12.0	16.0	V
Supply Current	I <sub>P</sub>	I <sub>18</sub> = −1.05mA	–	36	44	mA
		I <sub>18</sub> = −3.388mA	–	40	49	mA
Internal Reference Voltage						
Internal Reference Voltage	V <sub>ref</sub>		6.0	6.25	6.5	V
Temperature Coefficient	TC	T <sub>A</sub> +20° to +100°C	–	–	±90	10 <sup>−6</sup> /K
Power Supply Ripple Rejection	PSRR	f = 1kHz Sinewave	60	75	–	dB
		f = 1MHz Sinewave	25	35	–	dB
Supply Voltage (Pin1) to Ensure all Internal Reference Voltages	V <sub>P</sub>		9.2	–	16	V
Composite Sync Input (AC–Coupled)						
Sync Amplitude of Video Input Signal (Pin9)	V <sub>i sync</sub>	Sync on Green	–	300	–	mV
Top Sync Clamping Level			1.1	1.28	1.5	V
Slicing Level Above Top Sync Level		R <sub>S</sub> = 50Ω	90	120	150	mV
Allowed Source Resistance for 7% Duty Factor	R <sub>S</sub>	V <sub>i sync</sub> > 200mV	–	–	1.5	kΩ
Differntial Input Resistance	r <sub>g</sub>	During Sync	–	80	–	Ω
Charging Current of Coupling Capacitor	I <sub>g</sub>	V <sub>g</sub> > 1.5V	1.3	2.0	3.0	μA
Vertical Sunc Integration Time to Generate Vertical Trigger Pulse	t <sub>int</sub>	f <sub>H</sub> = 31kHz, I <sub>18</sub> = −1.050mA	7	10	13	μs
		f <sub>H</sub> = 64kHz, I <sub>18</sub> = −2.169mA	3.5	5.0	6.5	μs
		f <sub>H</sub> = 100kHz, I <sub>18</sub> = −3.388mA	2.5	3.4	4.5	μs
Horizontal Sync Input (DC–Coupled, TTL–Compatible)						
Sync Input Signal (Peak–to–Peak Value, Pin9)	V <sub>i sync</sub>		1.7	–	–	V
Slicing Level			1.2	1.4	1.6	V
Minimum Pulse Width	t <sub>p</sub>		700	–	–	ns
Rise Time and Fall Time	t <sub>r</sub> , t <sub>f</sub>		10	–	500	ns
Input Current	I <sub>g</sub>	V <sub>g</sub> = 0.8V	–	–	−200	μA
		V <sub>g</sub> = 5.5V	–	–	10	μA
Automatic Horizontal Polarity Switch						
Horizontal Sync Pulse Width Related to t <sub>H</sub> (Duty factor for Automatic Polarity Correction)	t <sub>p H</sub> /t <sub>H</sub>		–	–	30	%
Delay Time for Changing Sync Polarity	t <sub>p</sub>		0.3	–	1.8	ms

**Electrical Characteristics (Cont'd):** ( $V_P = 12V$ ,  $T_A = +25^\circ C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Vertical Sync Input (DC–Coupled, TTL–Coupled) (V–sync on Pin10)						
Sync Input Signal (Peak–to–Peak Value, Pin10)	$V_{i\ sync}$		1.7	–	–	V
Slicing Level			1.2	1.4	1.6	V
Input Current	$I_{10}$	$0 < V_{10} < 5.5V$	–	–	$\pm 10$	$\mu A$
Maximum Vertical Sync Pulse Width for Automatic Vertical Polarity Switch	$t_{p\ V}$		–	–	300	$\mu s$
Horizontal Clamping/Blanking Generator Output						
Output Voltage LOW	$V_8$		–	–	0.9	V
Blanking Output Voltage		Internal V Blanking	1.6	1.9	2.2	V
Clamping Output Voltage		H–Sync on Pin9	5.15	5.4	5.65	V
Internal Sink Current for All Output Levels	$I_8$	H and V Scanning	2.3	2.9	3.5	mA
External Load Current			–	–	–3.0	mA
Clamping Pulse Start	$t_8$		With End of H–Sync			
Clamping Pulse Width	$t_{clp}$	$V_8 = 3V$	0.6	0.8	1.0	$\mu s$
Steepness of Rise an Fall Times	S		–	60	75	ns/V
Vertical Oscillator						
Vertical Free–Running Frequency	$f_0$	$R_{15} = 22k\Omega$ , $C_{16} = 0.1\mu F$	–	42	–	Hz
Nominal Vertical Sync Range	$f_v$	No $f_0$ Adjustment	50	–	110	Hz
Voltage on Pin15	$V_{15}$	$R_{15} = 22k\Omega$	2.8	3.0	3.2	V
Delay Between Sync Pulse and Start of Vertical Scan	$t_d$	Measured on Pin8	240	300	360	$\mu s$
Control Current for Amplitude Control	$I_{12}$		–	$\pm 200$	–	$\mu A$
Capacitor for Amplitude Control	$C_{12}$		–	–	0.18	$\mu F$
Vertical Differential Output						
Differential Output Current Between Pin5 and Pin6 (Peak–to–Peak Value)	$I_o$	Mode 3, $I_{13} > -135\mu A$ , $R_{15} = 22k\Omega$	0.9	1.0	1.1	mA
Maximum Offset–Current Error		$I_o = 1mA$	–	–	$\pm 2.5$	%
Maximum Linearity Error			–	–	$\pm 1.5$	%
Vertical Amplitude Adjustment (In Percentage of Output Signal)						
Input Voltage	$V_{13}$		–	5.0	–	V
Adjustment Current	$I_{13}$	$I_o\ max\ (100\%)$	–110	–120	–135	$\mu A$
		$I_o\ min\ (Typically\ 58\%)$	–	0	–	$\mu A$
Horizontal Comparator PLL1						
Upper Control Voltage Limitation	$V_{17}$		–	5.9	–	V
Lower Control Voltage Limitation			–	5.1	–	V
Control Current	$I_{17}$		–	$+0.083I_{18}$	–	mA

**Electrical Characteristics (Cont'd):** ( $V_P = 12V$ ,  $T_A = +25^\circ C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Horizontal Oscillator						
Center Frequency	f <sub>OSC</sub>	R <sub>18</sub> = 2.4Ω (Pin18), C <sub>19</sub> = 10nF (Pin19)	–	31.45	–	kHz
Deviation of Center Frequency			–	–	±3	%
Temperature Coefficient			0	±200	±300	100 <sup>-6</sup> /K
Relative Holding/Catching Range	φ <sub>H</sub> /t <sub>H</sub>		±6	±6.5	±7.3	%
External Oscillator Current	I <sub>18</sub>		–0.5	–	–4.3	mA
Voltage at Reference Current Input	V <sub>18</sub>		2.35	2.5	2.65	V
Horizontal PLL2						
Upper Clamping Level of Flyback Input	V <sub>2</sub>	I <sub>2</sub> = 6mA	–	5.5	–	V
Lower Clamping Level of Flyback Input		I <sub>2</sub> = –1mA	–	–0.75	–	V
H–Flyback Slicing Level			–	3.0	–	V
Delay Between Midle of Sync and Middle of H–Flyback Related to t <sub>H</sub>	t <sub>d</sub> /t <sub>H</sub>		–	3.0	–	%
Upper Control Voltage Limitation	V <sub>20</sub>		–	6.2	–	V
Lower Control Voltage Limitation			–	4.8	–	V
Control Current	I <sub>20</sub>		–	±0.083I <sub>18</sub>	–	μA
PLL2 Control Range Related to t <sub>H</sub>	Δt/t <sub>H</sub>		30	–	–	%
Horizontal Output (Open–Collector)						
Output Voltage LOW	V <sub>3</sub>	I <sub>3</sub> = 20mA	–	–	0.3	V
		I <sub>3</sub> = 60mA	–	–	0.8	V
t <sub>H</sub> Duty factor	t <sub>p</sub> /t <sub>H</sub>		42	45	48	%
Threshold to Activate Under Voltage Protection	V <sub>P</sub>	Horizontal Output Off	–	5.6	–	V
		Horizontal Output On	–	5.8	–	V
Jitter of Horizontal Output	Δt <sub>H</sub>	f = 31kHz	–	–	3.5	ns
		f = 64kHz	–	–	1.9	ns
		f = 100kHz	–	–	1.2	ns
E/W Output (Note 2)						
Bottom Output Signal During Mid–Scan (Pin11)	V <sub>11</sub>	Internally Stabilized	1.05	1.2	1.35	V
Top Output Signal During Flyback			4.2	4.5	4.8	V
Temperature Coefficient of Output Signal			–	–	250	10 <sup>-6</sup> /K

Note 2. Parabola amplitude does not track with vertical amplitude adjustment. Tracking can be achieved by a resistor from vertical amplitude potentiometer to Pin14.

**Electrical Characteristics (Cont'd):** ( $V_P = 12V$ ,  $T_A = +25^{\circ}C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Internal Reference Voltage						
Input Voltage (Pin14)	$V_{14}$		–	5.0	–	V
Adjustment Current	$I_{14}$	100% Parabola	–110	–120	–135	$\mu A$
		Typically 28% Parabola	–	0	–	$\mu A$

**Pin Configuration Diagram**

