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NTE7174
Integrated Circuit
Quad EIA−422 Line Receiver
With Three−State Outputs

Description:

The NTE7174 is a Quad EIA−422/3 Receiver in a 16−Lead DIP type package that features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. The Receiver outputs are 74LS compatible, three−state structures which are forced to a high impedence state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margain and discourage output instability for slowly changing input waveforms.

Features:

- Four Independent Receiver Chains
- Three−State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis − 30mV (Typ) @ Zero Volts Common Mode
- Fast Propagation Times − 25ns (Typ)
- TTL Compatible
- Single 5V Supply Voltage

Absolute Maximum Ratings:

Power Supply Voltage, V_{CC} 8.0V
Input Common Mode Voltage, V_{ICM} . . . . . ±15
Input Differential Voltage, V_{ID} . . . . . ±25
Three−State Control Input Voltage, V_I 8.0Vdc
Output Sink Current, I_O 50mA
Storage Temperature Range, T_{stg} . . . . . −65° to +150°C
Operating Junction Temperature, T_J . . . . . +150°C

Recommended Operating Conditions:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}		4.75	−	5.25	V
Operating Ambient Temperature	T_A		0	−	70	°C
Input Common Mode Voltage	V_{ICR}		−7	−	+7	V
Input Differenctial Voltage	V_{IDR}		−	6	−	V

Electrical Characteristics: (T_A = +25°C, V_{CC} = 5V and V_{IK} = 0V, Note 1, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Voltage − High Logic State	V_{IH}	Three−State Control		2.0	−	−	V
Input Voltage − Low Logic State	V_{IL}	Three−State Control		−	−	0.8	V
Differential Input Threshold Voltage	$V_{TH(D)}$	−7V ≤ V_{IC} ≤ +7V, V_{IH} = 2V, Note 2	I_O = −0.4mA, V_{OH} ≥ 2.7V	−	−	0.2	V
			I_O = 8.8mA, V_{OH} ≥ 0.5V	−	−	−0.2	V
Input Bias Current	$I_{IB(D)}$	V_{CC} = 0V or 5.25V Other Inputs at 0V	V_I = −10V	−	−	−3.25	mA
			V_I = −3V	−	−	−1.50	mA
			V_I = +3V	−	−	+1.50	mA
			V_I = +10V	−	−	+3.25	mA
Input Balance and Output Level	V_{OH}	−7V ≤ V_{IC} ≤ 7.0, V_{IH} = 2V, Note 3	I_O = −0.4mA, V_{ID} =+0.4mA	2.7	−	−	V
	V_{OL}		I_O = 8.0mA, V_{ID} = −0.4V	−	−	0.5	V
Output Third State Leakage Current	I_{OZ}	$V_{(ID)}$ = +3.0V, V_{IL} = 0.8V, V_{OL} = 0.5V		−	−	−40	μA
		$V_{(ID)}$ = −3.0V, V_{IL} = 0.8V, V_{OH} = 2.7		−	−	40	μA
Output Short−Circuit Current	I_{OS}	$V_{I(D)}$ = 3.0V, V_{IH} = 2.0V, V_O = 0V, Note 4		−15	−	−100	mA
Input Current − Low Logic State	I_{IL}	Three−State Control, V_{IL} = 0.5V		−	−	−100	μA
Input Current − High Logic State	I_{IH}	Three−State Control, V_{IH} = 2.7V		−	−	20	μA
		Three−State Control, V_{IH} = 5.25V		−	−	100	μA
Input Clamp Diode Voltage	V_{IK}	Three−State Control, I_{Ik} = −10mA		−	−	−1.5	V
Power Supply Current	I_{CC}	V_{IL} = 2.0V		−	−	85	mA

Note 1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.

Note 2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.

Note 3. Refer to EIA−422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.

Note 4. Only one output at a time should be shorted.

Pin Connection Diagram