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RoHS 2002/95/EC

NTE7228
Integrated Circuit
Fixed Multi–Output Positive Voltage Regulator
10–Lead SIP

Description:

The NTE7228 is a multi–output positive voltage regulator in a 10–Lead SIP type package designed to provide fixed precision output voltages of 5.1V & 8V at current up to 0.5A and 12V at current up to 1A with an external PNP transistor. An internal reset circuit generates a reset pulse when Output 1 decreases below the regulated value. Output 2 and Output 3 can be disabled by TTL input. Protection features include over voltage protection, short circuit protection and thermal shutdown.

Features:

- Output Currents up to 0.5A (Output 1 & Output 2)
- Output Current up to 1A with External Transistor (Output 3)
- Fixed Precision Output 1 Voltage 5.1V ±2%
- Fixed Precision Output 2 Voltage 8V ±2%
- Control Signal Generator for Output 3 Voltage (12V ±2%)
- Reset Facility for Output Voltage 1
- Output 2 and Output 3 with Disable by TTL Input
- Current Limit Protection at Each Output
- Thermal Shutdown

Absolute Maximum Ratings:

DC Input Voltage, V_{IN} 20V
Disable Input Voltage, V_C 20V
Output Current, I_O 0.5A
Power Dissipation (No Heatsink), P_D 1.5W
Junction Temperature, T_J . . . . +150°C
Operating Temperature Range, T_{opr} . . . . 0° to +125°C

Electrical Characteristics: ($V_{IN}1$ = 7.5V, $V_{IN}2$ = 10.5V, T_J = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Output Voltage 1	V_O1	7.5V < $V_{IN}1$ < 14V	I_O1 = 10mA	5.0	5.1	5.2	V
			5mA < I_O1 < 500mA	4.9	5.1	5.3	V
Output Voltage 2	V_O2	10.5V < $V_{IN}2$ < 18V	I_O2 = 10mA	7.84	8.0	8.16	V
			5mA < I_O2 < 500mA	7.7	8.0	8.3	V
Dropout Output Voltage	V_D1	I_O1 = 500mA		–	–	2.5	V
	V_D2	I_O2 = 500mA		–	–	2.5	V
Line Regulation	$\pm V_O1$	$I_O1 = I_O2$ = 200mA	7.5V < $V_{IN}1$ < 14V	–	–	50	mV
	$\pm V_O2$		10.5V < $V_{IN}2$ < 18V	–	–	80	mV
Load Regulation	$\pm V_O1$	5mA < I_O1 < 500mA		–	–	100	mV
	$\pm V_O2$	5mA < I_O1 < 500mA		–	–	160	mV
Output Voltage 3	V_O3	V_{SYS} = 13V, I_O3 = 100mA		11.7	12.0	12.3	V
Line Regulation 3	$\pm V_O3$	13V < $V_{IN}2$ < 18V, I_O3 = 100mA		–	–	120	mV
Load Regulation 3	$\pm V_O3$	5mA < I_O3 < 1A		–	–	250	mV
Reset Pulse Delay	T_{rd}	C_D = 100nF, Note 1		–	25	–	ms
Saturation Voltage in Reset Condition	V_rL	I_6 = 5mA		–	–	0.4	V
Leakage Current at Pin6	I_rH	V_6 = 10V		–	–	10	° A
Output Voltage Thermal Drift	ST_t	0° < T_J < +125°C, Note 2		–	100	–	ppm/°C
Short Circuit Output Current	$I_{SC}1$	$V_{IN}1$ = 7.5V		–	–	1.6	A
	$I_{SC}2$	$V_{IN}2$ = 10.5V		–	–	1.6	A
Disable Voltage, High	$V_{dis}H$	Output 2 Active		2	–	–	V
Disable Voltage, Low	$V_{dis}L$	Output 2 Disabled		–	–	0.8	V
Disable Bias Current	I_{dis}	0V < V_{dis} < 7V		–100	–	2	° A
Junction Temperature for TSD	T_{tsd}	Note 2		–	145	–	°C
Quiescent Current	I_q	I_O1 = 10mA, Output 2 Disabled		–	–	2	mA
Reset Threshold Voltage	V_r	K = V_O1		K–0.4	K–0.25	K–0.1	V
Reset Threshold Hysteresis	V_{rth}	Note 1		20	50	100	mA

Note 1. To check the reset circuit, the reset output is low to discharge the delay capacitor (= C_D). If it's less than V_O1–0.25V. And the reset output is high when the delay capacitor voltage linearly increased by the internal current source (10° A) if it's more than V_O1 –0.2V. The equations of delay time is the same as below. T_{rd} = (C_D x 2.5) / 10° A.

Note 2. These parameters, although guaranteed, are not 100% tested in production.

Pin Connection Diagram

(Front View)