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NTE7238 & NTE7238SM
Integrated Circuit
Video Sync Separator

Description:

The NTE7238 (8–Lead DIP) and NTE7238SM (SIOC–8) video sync separators extract timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative going sync NTSC, PAL(Note 1), and SECAM video signals with amplitude from 0.5V to $2V_{p-p}$. These integrated circuits are also capable of providing sync separation for non–standard, faster horizontal rate video signals. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the externally set delay period, such as might be the case fo a non–standard video signal.

Features:

- AC Coupled Composite Input Signal
- > 10kΩ Input Resistance
- < 10mA Power Supply Drain Current
- Composite Sync and vertical Outputs
- Odd/Even Field Output
- Burst Gate/Back Porch Output
- Horizontal Scan Rates to 150kHz
- Edge Triggered Vertical Output
- Default Triggered Vertical Output for Non–Standard Video Signal (Video Games–Home Computers)

Absolute Maximum Ratings: (Note 2)

Supply Voltage	13.2V
Input Voltage (V_{CC} = 5V)	$3V_{p-p}$
Input Voltage ($V_{CC} \geq 8V$)	$6V_{p-p}$
Output Sink Currents, Pin1, Pin3, and Pin5	5mA
Output Sink Current, Pin7	2mA
Package Dissipation (Note 3)	1100mW
Storage Temperature Range	–65° to +150°C

Note 1. PAL in this datasheet refers to European broadcast TV standard “Phase Alternating Line”, and not to Programmable Array Logic.

Note 2. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.

Note 3. For operation in ambient temperatures above +25°C, the device must be derated based on a +150°C maximum junction temperature an a package thermal resistance of 110°C/W, junction–to–ambient.

RoHS 2002/95/EC

Absolute Maximum Ratings (Cont'd): (Note 2)

ESD Susceptibility (Note 4) 2kV
ESD Susceptibility (Note 5) 200V
Soldering Information, 8−Lead DIP . . . . . +260°C
Soldering Information, SOIC−8
Vapor Phase (60sec) . . . . . +215°C
Infrared (15sec) . . . . . +220°C

Note 2. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed.

Note 4. ESD susceptibility test uses the "human body model, 100pF discharged through a 1.5kΩ resistor".

Note 5. Machine Model, 220pF − 240pF discharged through all pins.

Electrical Characteristics: (V_{CC} = 5V, R_{SET} = 680kΩ, T_A = 0° to +70°C by correlation with 100% electrical testing at T_A = +25°C, Note 6)

Parameter	Test Conditions		Min	Typ	Max	Unit
Supply Current	Outputs at Logic 1	V_{CC} = 5V	−	5.2	10	mA
		V_{CC} = 12V	−	5.5	12	mA
DC Input Voltage	Pin2		1.3	1.5	1.8	V
Input Threshold Voltage	Note 7		55	70	85	mV
Input Discharge Current	Pin2, V_{IN} = 2V		6	11	16	μA
Input Clamp Charge Current	Pin2, V_{IN} = 1V		0.2	0.8	−	mA
R_{SET} Pin Reference Voltage	Pin6, Note 8		1.10	1.22	1.35	V
Composite Sync & Vertical Outputs	I_{OUT} = 40μA, Logic 1	V_{CC} = 5V	4.0	4.5	−	V
		V_{CC} = 12V	11.0	−	−	V
	I_{OUT} = 1.6mA, Logic 1	V_{CC} = 5V	2.4	3.6	−	V
		V_{CC} = 12V	10.0	−	−	V
Burst Gate & Odd/Even Outputs	I_{OUT} = 40μA, Logic 1	V_{CC} = 5V	4.0	4.5	−	V
		V_{CC} = 12V	11.0	−	−	V
Composite Sync Output	I_{OUT} = −1.6mA, Logic 0, Pin1		−	0.2	0.8	V
Vertical Sync Output	I_{OUT} = −1.6mA, Logic 0, Pin3		−	0.2	0.8	V
Burst Gate Output	I_{OUT} = −1.6mA, Logic 0, Pin5		−	0.2	0.8	V
Odd/Even Output	I_{OUT} = −1.6mA, Logic 0, Pin7		−	0.2	0.8	V
Vertical Sync Width			190	230	300	μs
Burst Gate Width	2.7kΩ from Pin5 to V_{CC}		2.5	4.0	4.7	μs
Vertical Default Time	Note 9		32	65	90	μs

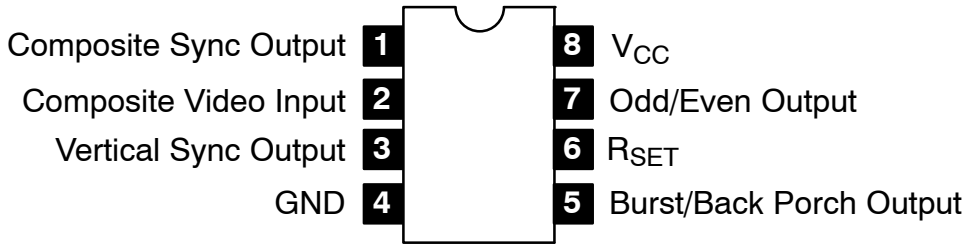
Note 6. Typicals are at T_J = +25°C and represent the most likely parametric norm.

Note 7. Relative difference between the input clamp voltage and the minimum input voltage which produces a horizontal output pulse.

Note 8. Careful attention should be made to prevent parasitic capacitance coupling from any output pin (Pins 1, 3, 5, and 7) to the R_{SET} pin (Pin6).

Note 9. Delay time between the start of vertical sync (at input) and the vertical output pulse.

Pin Connection Diagram



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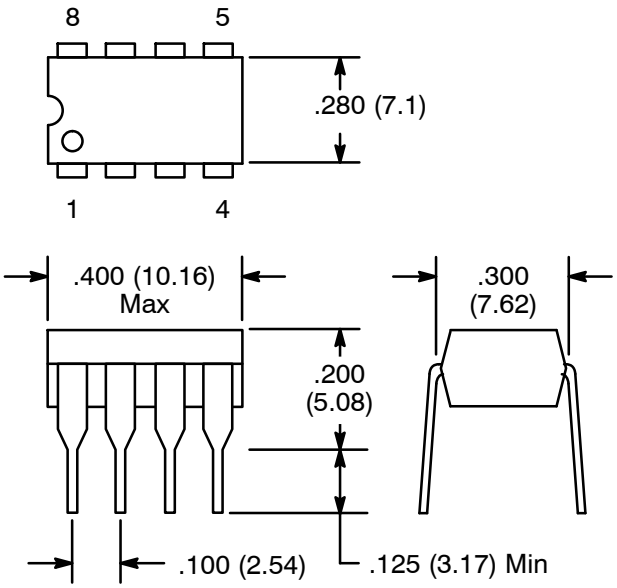

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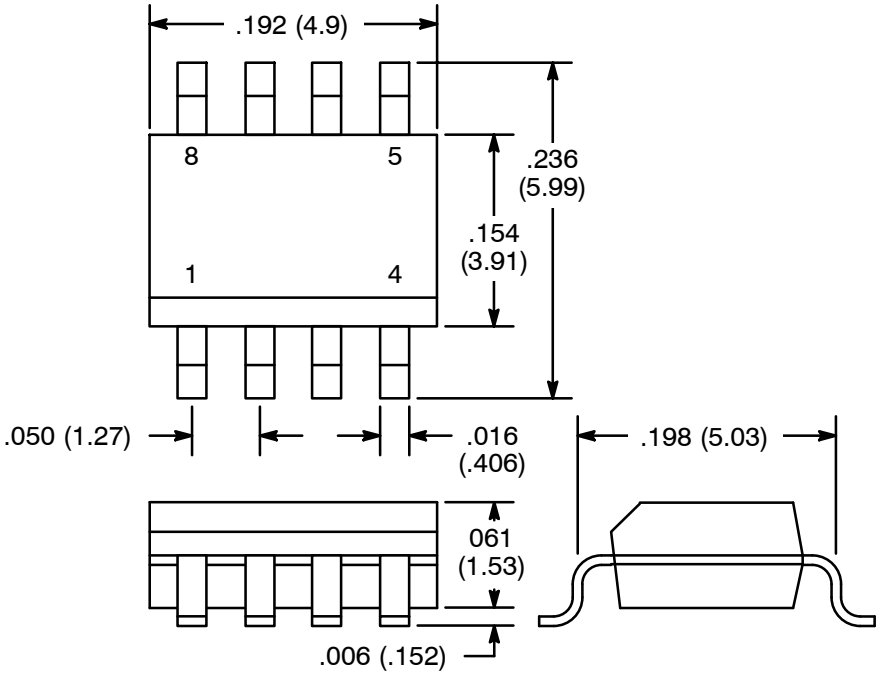

NOTE: Pin1 on Beveled Edge