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## NTE74LS374 Integrated Circuit TTL- Octal D-Type Edge-Triggered Flip-Flop with 3-State Outputs

**Description:**

The NTE74LS374 is an octal D-type flop-flop in a 20-Lead DIP type package that features three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provides the capability of being connected directly to and driving the bus lines in a bus-organized system without the need for interface or pull-up components. The NTE74LS374 is particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

**Features:**

- 8 D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs

**Absolute Maximum Ratings:** (Note 1)

Supply Voltage, $V_{CC}$ .....	7V
Input Voltage, $V_{IN}$ .....	7V
Off-State Output Voltage, $V_{OZ}$ .....	5.5V
Operating Temperature Range, $T_A$ .....	0°C to +70°C
Storage Temperature Range, $T_{stg}$ .....	-65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

**Recommended Operating Conditions:**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.75	5.0	5.25	V
High-Level Output Voltage	$V_{OH}$	–	–	5.5	V
High-Level Output Current	$I_{OH}$	–	–	–2.6	mA
Low Level Output Current	$I_{OL}$	–	–	24	mA
Pulse Duration CLK High	$t_w$	15	–	–	ns
CLK Low		15	–	–	ns
Data Setup Time	$t_{su}$	20↑	–	–	ns
Data Hold Time (Note 2)	$t_h$	0↑	–	–	ns
Operating Temperature Range	$T_A$	0	–	+70	°C

Note 2. The  $t_h$  specification applies only for data frequency below 10MHz. Designs above 10MHz should use a minimum of 5ns.

**Electrical Characteristics:** (Note 3, Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
High Level Input Voltage	$V_{IH}$		2	–	–	V	
Low Level Input Voltage	$V_{IL}$		–	–	0.8	V	
Input Clamp Voltage	$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$	–	–	–1.5	V	
High Level Output Voltage	$V_{OH}$	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	2.4	3.1	–	V	
Low Level Output Voltage	$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2\text{V}, V_{IL} = \text{MAX}$	$I_{OL} = 12\text{mA}$	–	0.25	0.4	V
			$I_{OL} = \text{MAX}$	–	0.35	0.5	V
Off-State Output Current	$I_{OZ}$	$V_{CC} = \text{MAX}, V_{IH} = 2\text{V}, V_{IL} = \text{MAX}$	$V_O = 2.7\text{V}$	–	–	20	$\mu\text{A}$
			$V_O = 0.4\text{V}$	–	–	–20	$\mu\text{A}$
Input Current	$I_I$	$V_{CC} = \text{MAX}, V_I = 7\text{V}$	–	–	0.1	mA	
High Level Input Current	$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$	–	–	20	$\mu\text{A}$	
Low Level Input Current	$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$	–	–	–0.4	mA	
Short-Circuit Output Current	$I_{OS}$	$V_{CC} = \text{MAX}, \text{Note 5}$	–30	–	–130	mA	
Supply Current	$I_{CC}$	$V_{CC} = \text{MAX}, \text{Output Control} = 4.5\text{V}$	–	27	40	mA	

Note 3. For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 4. All typical values are at  $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$ .

Note 5. Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

**AC Electrical Characteristics:** ( $V_{CC} = 5\text{V}, T_A = +25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	$f_{\text{max}}$	$C_L = 45\text{pF}, R_L = 667\Omega,$ Note 6	35	50	–	MHz
Propagation Delay Time (Clock or Enable Input to Any Q Output)	$t_{PLH}$		–	15	28	ns
	$t_{PHL}$		–	19	28	ns
Output Enable Time (Output Control Input to Any Q Output)	$t_{PZH}$		–	20	26	ns
	$t_{PZL}$	–	21	36	ns	
Output Disable Time (Output Control Input to Any Q Output)	$t_{PHZ}$	$C_L = 5\text{pF}, R_L = 667\Omega$	–	15	28	ns
	$t_{PLZ}$		–	12	20	ns

Note 6. Maximum clock frequency is tested with all outputs loaded.

**Function Table:**

Output Enable	Enable Latch	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

**Pin Connection Diagram**

