

## NTE9370 Integrated Circuit HTL, Quad D-Type Flip-Flop

### **Description:**

Four D-type flip-flops utilizing a common clock line make up the NTE9370. Each flip-flop has complementary passive pull up outputs with a single D input. This circuit is ideal as a quad latch for temporary storage of 4-bit binary numbers.

Data is transferred from D inputs to outputs when the clock line is low. With the clock line high, output data is held and D inputs are ignored.

### **Absolute Maximum Ratings:**

Supply Voltage:

Continuous ..... 16.5V  
Pulsed (< 0.1sec) ..... 18V

Input Voltage ..... -0.5V to 16.5V

Voltage Applied to Output ..... -0.5V to +16.5V

Continuous Sink Current ( $T_A = +25^\circ\text{C}$ ):

Continuous ..... 15mA  
Surge (< 1sec) ..... 20mA

Output Short Circuit Duration to GND ..... Continuous

Operating Temperature Range,  $T_{opr}$  .....  $-30^\circ$  to  $+85^\circ\text{C}$

Storage Temperature Range,  $T_{stg}$  .....  $-55^\circ$  to  $+100^\circ\text{C}$

Lead Temperature (During Soldering, 1/16" from case, 10sec max),  $T_L$  .....  $+300^\circ\text{C}$

### **Electrical Characteristics:** ( $V_{CC} = 12V \pm 1V$ unless otherwise specified)

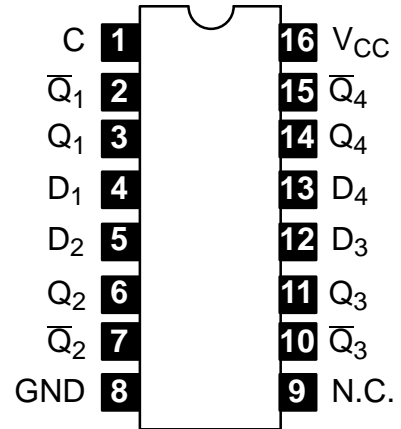
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Threshold Voltage, Low	$V_{IL}$	Guaranteed input low threshold for all inputs	5	—	—	V
Input Threshold Voltage, High	$V_{IH}$	Guaranteed input high threshold for all inputs	—	—	6.5	V
Input Current, Low (1 Unit Load)	$I_{IL}$	$V_{CC} = \text{Max}$ , $V_{IN} = V_{OL1} \text{ max}$	—	—	2.1	mA
Input Leakage Current (1 Unit Load)	$I_{IH}$	$V_{CC} = \text{Max}$ , $V_{IN} = V_{CC}$	—	—	10	$\mu\text{A}$
Output Low Voltage	$V_{OL}$	$V_{CC} = \text{Min}$ , $V_{IL} = 5V$ $V_{IH} = 6.5V$ , $I_{OL} = \text{F.O.} \times \text{U.L.}$	—	—	1.5	V
Output High Voltage	$V_{OH}$		10	—	—	V
Test Supply Voltage	$V_{CC}$		11	12	13	V

Note 1. F.O. is fanout in unit loads (U.L.). A unit load is defined by the above input specifications.

**Truth Table**

C	D	$Q^{n+1}$
1	1	$Q^n$
1	0	$Q^n$
0	1	1
0	0	0

**Pin Connection Diagram**



<u>Pins</u>	<u>Function</u>	<u>Loading</u>
D	Data Inputs	2 UL
C	Clock Input	1 UL
$Q, \overline{Q}$	Outputs	5 UL at 1.5V

