NTE985
Integrated Circuit
TV Luminance Processor

Description:
The NTE985 is a monolithic silicon integrated circuit that performs the luminance processing functions of amplification; contrast, brightness and peaking control; blanking; and black-level clamping.

Features:
- Black-Level Clamping
- Linear DC Controls for Brightness, Contrast and Peaking
- Horizontal and Vertical Blanking
- “Hermetic Chip” Construction
- Silicon Nitride Passivated
- Platinum Silicide Ohmic Contacts
- Operates with Standard or Tapped Delay Line

Absolute Maximum Ratings:
DC Supply Current .................................................. 57mA
Device Dissipation:
  Up to $T_A = +55^\circ C$ ............................................ 750mW
  Above $T_A = +55^\circ C$ ............................................ derate linearly 7.9mW/°C
Operating Ambient Temperature Range, $T_A$ .................................... $-40^\circ C$ to $+85^\circ C$
Storage Temperature Range, $T_{stg}$ ........................................ $-65^\circ C$ to $+150^\circ C$
Lead Temperature (During Soldering, 1/16” ±1/32” from case, 10sec max), $T_L$ ............ $+265^\circ C$
Electrical Characteristics: \((T_A = +25°C\) unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Bias Volts</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage At Term. 13</td>
<td>6.5</td>
<td>S1 2 1 1 1 1 2 2 4 1 1 2 1 1 1 1 2 1 1 11 12.3 13.2</td>
<td>V</td>
<td></td>
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<tr>
<td>Quiescent Voltage At Term. 4</td>
<td>6.5</td>
<td>S1 2 1 1 1 1 2 2 3 1 1 2 1 1 1 1 1 3.3 4 5.7</td>
<td>V</td>
<td></td>
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<tr>
<td>Quiescent Voltage At Term 7</td>
<td>6.5</td>
<td>S1 2 1 1 1 1 2 2 2 1 2 1 2 1 1 1 1 7.1 7.7 8.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Current into Term. 13 (Term 13 Connected</td>
<td>6.5</td>
<td>S1 2 1 1 1 1 2 2 3 1 1 2 1 2 1 2 1 1 10 18 30</td>
<td>mA</td>
<td></td>
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</tbody>
</table>

**Static Characteristics**

- **Note 1**: Set 50kHz generator for 200mV_{rms}. Adjust R1 Peaking control for minimum setting, measure wide-band gain at terminal 7.
- **Note 2**: Set 50kHz generator for 200mV_{rms}. Adjust R1 for minimum setting, measure contrast gain reduction at terminal 7.
- **Note 3**: Set 50kHz generator for 200mV_{rms}. Adjust R1 for minimum setting, measure peaking gain reduction at terminal 7.
- **Note 4**: Adjust R1 for minimum setting. With S2 at switch position 1 and S7 at switch position 3, set 50kHz generator for 3.8V_{p−p}. Then with S2, set 1MHz generator for 200mV_{rms}. Then with S7 at switch position 2, measure downward modulation of the 1MHz signal due to the 50kHz signal.

\[
\text{Modulated I−MHz Signal} = \frac{B−A}{B}
\]

- **Note 5**: Repeat step 4 except that the 50kHz generator must be set at 5V_{p−p}.

**Dynamic Characteristics**

- **Wide-Band Gain (Note 1)**: 7.3 1 1 1 1 2 1 1 1 1 2 2 1 1 1 1 1 3 5 dB
- **Contrast Gain Reduction (Note 2)**: 7.3 1 1 1 1 2 1 1 1 1 2 2 1 1 1 1 1 27 30 dB
- **Peaking Gain (Note 1)**: 7.3 1 1 1 1 2 1 1 1 1 2 2 1 1 1 1 1 9 13 17 dB
- **Peaking Gain Reduction (Note 3)**: 7.3 1 1 1 1 2 1 1 1 1 2 2 1 1 1 1 1 16 18 dB
- **Max. Intermodulation Distortion 3.8V (Note 4)**: 7.3 1 1 1 1 1 2 2 2 1 1 1 1 1 1 1 1 20 40 %
- **5V (Note 5)**: 7.3 1 1 1 1 1 2 2 2 1 1 1 1 1 1 1 1 40 40 %

**Pin Connection Diagram**

- Video Input: 1, N.C.
- Peaking Input: 2, 15, N.C.
- Peaking Input: 3, N.C.
- Video Output: 4, 13, Shunt Reg and Bias
- Substrate: 5, 12, Clamp Inhibit Input
- Clamp Input: 6, 11, Peaking Control
- Clamp Video Output: 7, 10, Contrast Control
- Blanking Input: 8, 9, Brightness Control