NTE2117
Integrated Circuit
16K Dynamic Random Access Memory (RAM)

Description:
The NTE2117 is a new generation MOS dynamic random access memory circuit in a 16–Lead DIP type package organized as 16,384 x 1–bit and incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving higher performance levels in both speed and power.

System oriented features include ±10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize “false triggering” of the inputs (a common cause of soft errors), on–chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of the memory system. The NTE2117 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read–modify–write cycles, this device is capable of delayed write cycles, page–mode operation, and RAS–Only refresh. Proper control of the clock inputs (RAS, CAS, and WRITE) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

Features:
- Fast Access Time: 200ns, 375ns cycle
- ±10% Tolerance on All Power Supplies (+12V, ±5V)
- Low Power: 462mW Active, 20W Standby (Max)
- Output Data Controlled bt CAS and Unlatched at End of Cycle to Allow Two Dimensional Chip Selection and Extended Page Boundary.
- Common I/O Capability using “Early Write” Operation
- Read–Modify–Write, RAS–Only Refresh, and Page–Mode Capability
- All Inputs TTL Compatible, Low Capacitance, and Protected Against Static Charge
- 128 Refresh Cycles
- ECL Compatible on VBB Power Supply (~5.7V)

Absolute Maximum Ratings: (Note 1)
Voltage on Any Pin Relative to VBB .......................... -0.5V to +20V
Voltage on VDD, VCC Supplies Relative to VSS .......................... -1V to +15V
VBB – VSS (VDD – VSS > 0V) ............................. 0V
Ambient Operating Temperature, TA .......................... 0° to +70°C
Storage Temperature Range, Tstg ............................. -55° to +125°C
Short–Circuit Output Current .......................................................... 50mA
Power Dissipation, PD ............................. 1W
Note 1. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operation Conditions:** \(0^\circ \leq T_A \leq +70^\circ\text{C}, \text{Note 2, Note 3 unless otherwise specified}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>V_DD</td>
<td></td>
<td>10.8</td>
<td>12.0</td>
<td>13.2</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V_CC (Note 4)</td>
<td></td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V_SS</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>V_BB</td>
<td></td>
<td>-4.5</td>
<td>-5.0</td>
<td>-5.7</td>
<td>V</td>
</tr>
<tr>
<td>Input High (Logic “1”) Voltage (RAS, CAS, WRITE)</td>
<td>V_IHC</td>
<td></td>
<td>2.4</td>
<td>-</td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>Input High (Logic “1”) Voltage (All Other Inputs)</td>
<td>V_IH</td>
<td></td>
<td>2.2</td>
<td>-</td>
<td>7.0</td>
<td>V</td>
</tr>
<tr>
<td>Input Low (Logic “0”) Voltage (All Inputs)</td>
<td>V_IL</td>
<td></td>
<td>-1.0</td>
<td>-</td>
<td>0.8</td>
<td>V</td>
</tr>
</tbody>
</table>

Note 2. Several cycles are required after power–up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

Note 3. All voltages referenced to V_SS.

Note 4. Output voltage will swing from V_SS to V_CC when activated with no current loading. For purposes of maintaining data in standby mode, V_CC may be reduced to V_SS without affecting refresh operations or data retention. However, the VOH (min) specification is not guaranteed in this mode.

**DC Electrical Characteristics:** \(0^\circ \leq T_A \leq +70^\circ\text{C}, V_{DD} = 12V \pm10\%, V_{CC} = 5V \pm10\%, V_{SS} = 0, -5.7V \leq V_{BB} \leq -4.5V unless otherwise specified\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Power Supply Operating Current</td>
<td>I_DD1</td>
<td>RAS, CAS Cycling, t_{RC} = t_{RC} Min</td>
<td>Note 5</td>
<td>-</td>
<td>-</td>
<td>35 mA</td>
</tr>
<tr>
<td></td>
<td>I_CC1</td>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>I_BB1</td>
<td></td>
<td></td>
<td>-</td>
<td>200</td>
<td>µA</td>
</tr>
<tr>
<td>Power Supply Standby Current</td>
<td>I_DD2</td>
<td>RAS = V_IHC, D_OUT = High Impedance</td>
<td>-</td>
<td>-</td>
<td>1.5</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>I_CC2</td>
<td></td>
<td></td>
<td>-</td>
<td>+10</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>I_BB2</td>
<td></td>
<td></td>
<td>-</td>
<td>100</td>
<td>µA</td>
</tr>
<tr>
<td>Average Power Supply Current, Refresh Mode</td>
<td>I_DD3</td>
<td>RAS Cycling, RAS = V_IHC, t_{RC} = t_{RC} Min</td>
<td>Note 5</td>
<td>-</td>
<td>-</td>
<td>25 mA</td>
</tr>
<tr>
<td></td>
<td>I_CC3</td>
<td></td>
<td></td>
<td>-</td>
<td>+10</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>I_BB3</td>
<td></td>
<td></td>
<td>-</td>
<td>200</td>
<td>µA</td>
</tr>
<tr>
<td>Average Power Supply Current, Page–Mode</td>
<td>I_DD4</td>
<td>RAS = V_IL, CAS Cycling, t_{PC} = t_{PC} Min</td>
<td>Note 5</td>
<td>-</td>
<td>-</td>
<td>27 mA</td>
</tr>
<tr>
<td></td>
<td>I_CC4</td>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>I_BB4</td>
<td></td>
<td></td>
<td>-</td>
<td>200</td>
<td>µA</td>
</tr>
<tr>
<td>Input Leakage Current (Any Input)</td>
<td>I_{(L)}</td>
<td>V_BB = -5V, 0V \leq V_{IN} \leq +7V, all other pins not under test = 0V</td>
<td>-10</td>
<td>-</td>
<td>+10</td>
<td>µA</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>I_{O(L)}</td>
<td>D_OUT is disabled, 0V \leq V_{OUT} \leq+5.5V</td>
<td>-10</td>
<td>-</td>
<td>+10</td>
<td>µA</td>
</tr>
<tr>
<td>Output High (Logic “1”) Voltage</td>
<td>V_OH</td>
<td>I_OUT = -5mA</td>
<td>2.4</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>Output Low (Logic “0”) Voltage</td>
<td>V_OL</td>
<td>I_OUT = 4.2mA</td>
<td>-</td>
<td>-</td>
<td>0.4</td>
<td>V</td>
</tr>
</tbody>
</table>

Note 5. I_DD1, I_DD3, and I_DD4 depend on cycle rate.
Note 6. \( I_{CC1} \) and \( I_{CC4} \) depend upon output loading. During readout of high level data \( V_{CC} \) is connected through a low impedance (135\( \Omega \) Typ) to data out. At all other times \( I_{CC} \) consists of leakage currents only.

**Electrical Characteristics and Recommended AC Operating Conditions:** \((0^\circ C \leq T_A \leq +70^\circ C,\ V_{DD} = 12V \pm 10\%,\ V_{CC} = 5V \pm 10\%,\ V_{SS} = 0V,\ -5.7V \leq V_{BB} \leq -4.5V,\ Note 2,\ Note 7,\ Note 8,\ Note 9\) unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random Read or Write Cycle Time</td>
<td>( t_{RC} )</td>
<td>Note 10</td>
<td>375</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Read–Write Cycle Time</td>
<td>( t_{RWC} )</td>
<td>Note 10</td>
<td>375</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Read–Modify–Write Cycle Time</td>
<td>( t_{RMW} )</td>
<td>Note 10</td>
<td>405</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Page Mode Cycle Time</td>
<td>( t_{PC} )</td>
<td>Note 10</td>
<td>225</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Access Time from RAS</td>
<td>( t_{RAC} )</td>
<td>Note 11, Note 13</td>
<td>–</td>
<td>–</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>Access Time from CAS</td>
<td>( t_{CAC} )</td>
<td>Note 12, Note 13</td>
<td>–</td>
<td>–</td>
<td>135</td>
<td>ns</td>
</tr>
<tr>
<td>Output Buffer Turn–Off Delay</td>
<td>( t_{OFF} )</td>
<td>Note 14</td>
<td>0</td>
<td>–</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Transition Time (Rise and Fall)</td>
<td>( t_{T} )</td>
<td>Note 9</td>
<td>3</td>
<td>–</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>RAS Precharge Time</td>
<td>( t_{RP} )</td>
<td></td>
<td>120</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>RAS Pulse Width</td>
<td>( t_{RAS} )</td>
<td></td>
<td>200</td>
<td>–</td>
<td>10,000</td>
<td>ns</td>
</tr>
<tr>
<td>RAS Hold Time</td>
<td>( t_{RSH} )</td>
<td></td>
<td>135</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>CAS Hold Time</td>
<td>( t_{CSH} )</td>
<td></td>
<td>200</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>CAS Pulse Width</td>
<td>( t_{CAS} )</td>
<td></td>
<td>135</td>
<td>–</td>
<td>10,000</td>
<td>ns</td>
</tr>
<tr>
<td>RAS to CAS Delay Time</td>
<td>( t_{RCD} )</td>
<td>Note 15</td>
<td>25</td>
<td>–</td>
<td>65</td>
<td>ns</td>
</tr>
<tr>
<td>CAS to RAS Precharge Time</td>
<td>( t_{CRP} )</td>
<td></td>
<td>–20</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Row Address Set–Up Time</td>
<td>( t_{ASR} )</td>
<td></td>
<td>0</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Row Address Hold Time</td>
<td>( t_{RASH} )</td>
<td></td>
<td>25</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Column Address Set–Up Time</td>
<td>( t_{ASC} )</td>
<td></td>
<td>–10</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Column Address Hold Time</td>
<td>( t_{CAH} )</td>
<td></td>
<td>55</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Column Address Hold Time Referenced to RAS</td>
<td>( t_{AR} )</td>
<td></td>
<td>120</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Read Command Set–Up Time</td>
<td>( t_{RCS} )</td>
<td></td>
<td>0</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Read Command Hold Time</td>
<td>( t_{RCH} )</td>
<td></td>
<td>0</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Write Command Hold Time</td>
<td>( t_{WCH} )</td>
<td></td>
<td>55</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Write Command Hold Time Referenced to RAS</td>
<td>( t_{WCR} )</td>
<td></td>
<td>120</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Write Command Pulse Width</td>
<td>( t_{WP} )</td>
<td></td>
<td>55</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Write Command to RAS Lead Time</td>
<td>( t_{RWL} )</td>
<td></td>
<td>70</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Write Command to CAS Lead Time</td>
<td>( t_{CWL} )</td>
<td></td>
<td>70</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Data–In Set–Up Time</td>
<td>( t_{DS} )</td>
<td>Note 16</td>
<td>0</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Data–In Hold Time</td>
<td>( t_{DH} )</td>
<td>Note 16</td>
<td>55</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Data–In Hold Time Referenced to RAS</td>
<td>( t_{DHR} )</td>
<td>Note 16</td>
<td>120</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>CAS Precharge Time (for Page–Mode Cycle Only)</td>
<td>( t_{CP} )</td>
<td></td>
<td>80</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>Refresh Period</td>
<td>( t_{REF} )</td>
<td></td>
<td>–</td>
<td>–</td>
<td>2</td>
<td>ms</td>
</tr>
<tr>
<td>WRITE Command Set–Up Time</td>
<td>( t_{WCS} )</td>
<td>Note 17</td>
<td>–20</td>
<td>–</td>
<td>–</td>
<td>ns</td>
</tr>
</tbody>
</table>
Note 7. $T_A$ is specified here for operation at frequencies to $t_{RC} \geq t_{RC} (\text{min})$. Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.

Note 8. AC measurements assume $t_T = 5\text{ns}$.

Note 9. $V_{IHC}(\text{min})$ or $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also transition times are measured between $V_{IHC}$ or $V_{IH}$ and $V_{IL}$.

Note 10. The specifications for $t_{RC}(\text{min})$, $t_{RMW}(\text{min})$, and $t_{RWC}(\text{min})$ are used only to indicate cycle time at which proper operation over the full temperature range ($0^\circ C \leq T_A \leq +70^\circ C$) is assured.

Note 11. Assumes that $t_{RCD} \leq t_{RCD}(\text{Max})$. If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds the value shown.

Note 12. Assumes that $t_{RCD}(\text{Max})$.

Note 13. Measured with a load equivalent to 2 TTL loads and 100pF.

Note 14. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Note 15. Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point if $t_{RCD}$ is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by $t_{CAC}$.

Note 16. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read–modify–write cycles.

Note 17. $t_{WCS}$, $t_{CWD}$, and $t_{RWD}$ are restrictive operating parameters in read write and read modify write cycles only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$, the cycle is a read–write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

**AC Electrical Characteristics:** ($0^\circ C \leq T_A \leq +70^\circ C$, $V_{DD} = 12\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $-5.7\text{V} \leq V_{BB} \leq -4.5\text{V}$ unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Capacitance ($A_0$ – $A_6$, $D_{IN}$)</td>
<td>$C_{i1}$</td>
<td>Note 18</td>
<td>4</td>
<td>5</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Input Capacitance RAS, CAS, WRITE</td>
<td>$C_{i2}$</td>
<td>Note 18</td>
<td>$\frac{\Delta t}{\Delta V}$</td>
<td>8</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance ($D_{OUT}$)</td>
<td>$C_O$</td>
<td>Note 18, Note 19</td>
<td>–</td>
<td>5</td>
<td>7</td>
<td>pF</td>
</tr>
</tbody>
</table>

Note 18. Effective capacitance calculated from the equation:

$$\Delta V \text{ with } \Delta = 3\text{V and power supplies at nominal levels.}$$

Note 19. $CAS = V_{IHC}$ to disable $D_{OUT}$.  

Parameter Unit MaxTypMin Test Conditions Symbol

CAS to WRITE Delay $t_{CWD}$ Note 17 80 – – ns

RAS to WRITE Delay $t_{RWD}$ Note 17 145 – – ns