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NTE4020B & NTE4020BT
Integrated Circuit
CMOS, 14–Bit Binary Counter

Description:

The NTE4020B (16–Lead DIP) and NTE4020BT (SOIC–16) are 14–stage binary counter devices constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. These devices are designed with an input wave shaping circuit and 14 stages of ripple–carry binary counter. The device advances the count on the negative–going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency–dividing circuits.

Features:

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from Stages 1 and 4 Through 14
- Common Reset Line

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C
Storage Temperature, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	µAdc
		15	–	20	–	0.015	20	–	600	µAdc
Total Supply Current	I_T	5.0	I_T = (0.42µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 3, Note 4)		10	I_T = (0.85µA/kHz) f + I_{DD}							µAdc
		15	I_T = (1.43µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ V_{fk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					
t_{TLH}, t_{THL} = (1.5ns/pf) C_L + 25ns		5.0	–	100	200	ns
t_{TLH}, t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{TLH}, t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time	t_{PLH}. t_{PHL}					
Clock to Q1						
t_{PLH}, t_{PHL} = (0.90ns/pf) C_L + 115ns		5.0	–	260	520	ns
t_{PLH}, t_{PHL} = (0.36ns/pf) C_L + 47ns		10	–	115	230	ns
t_{PLH}, t_{PHL} = (0.26ns/pf) C_L + 37ns		15	–	80	160	ns
Clock to Q14						
t_{PLH}, t_{PHL} = (0.90ns/pf) C_L + 115ns		5.0	–	1820	3900	ns
t_{PLH}, t_{PHL} = (0.36ns/pf) C_L + 47ns		10	–	805	1725	ns
t_{PLH}, t_{PHL} = (0.26ns/pf) C_L + 37ns		15	–	560	1200	ns
Propagation Delay Time	t_{PHL}					
Reset to Q_n						
t_{PHL} = (1.7ns/pf) C_L + 285ns		5.0	–	370	740	ns
tt_{PHL} = (0.66ns/pf) C_L + 122ns		10	–	155	310	ns
t_{PHL} = (0.5ns/pf) C_L + 90ns		15	–	115	230	ns
Clock Pulse Width	t_{WH}	5.0	500	140	–	ns
		10	165	55	–	ns
		15	125	38	–	ns
Clock Pulse Frequency	f_{CL}	5.0	–	2.0	1.0	MHz
		10	–	6.0	3.0	MHz
		15	–	8.0	4.0	MHz
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			–
		10				–
		15				–
Reset Pulse Width	t_{WL}	5.0	3000	320	–	ns
		10	550	120	–	ns
		15	420	80	–	ns
Reset Removal Time	t_{rem}	5.0	130	65	–	ns
		10	50	25	–	ns
		15	30	15	–	ns

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

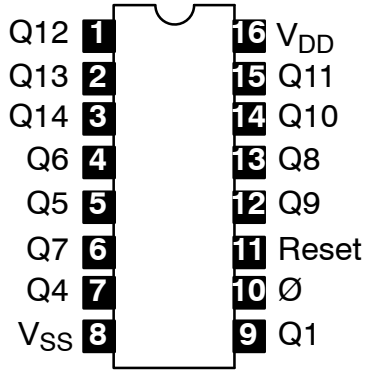
Note 3. The formulas given are for the typical characteristics only at +25°C.

Truth Table

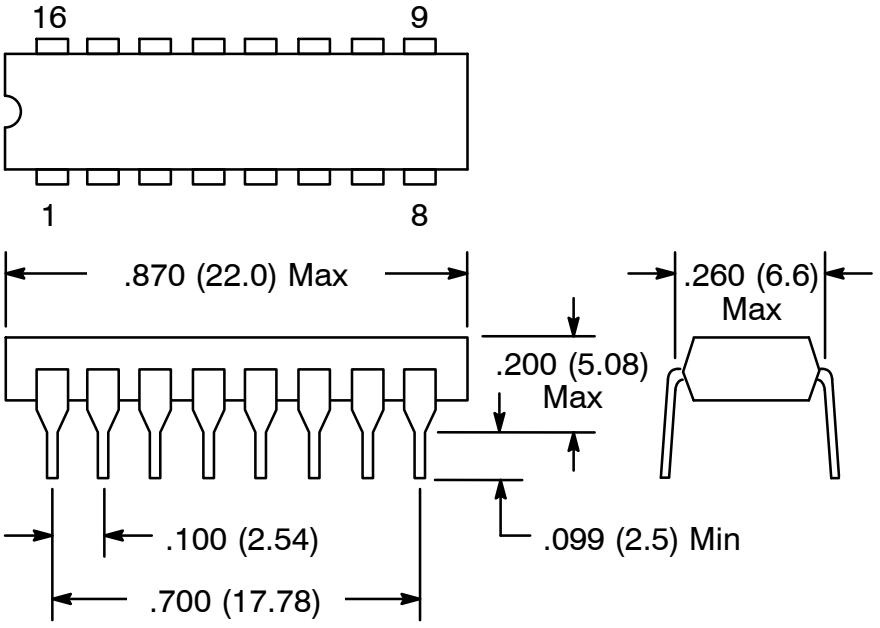
CLOCK	Reset	Output State
	0	No Change
	0	Advance to Next State
X	1	All Outputs are Low

X = Don’t care

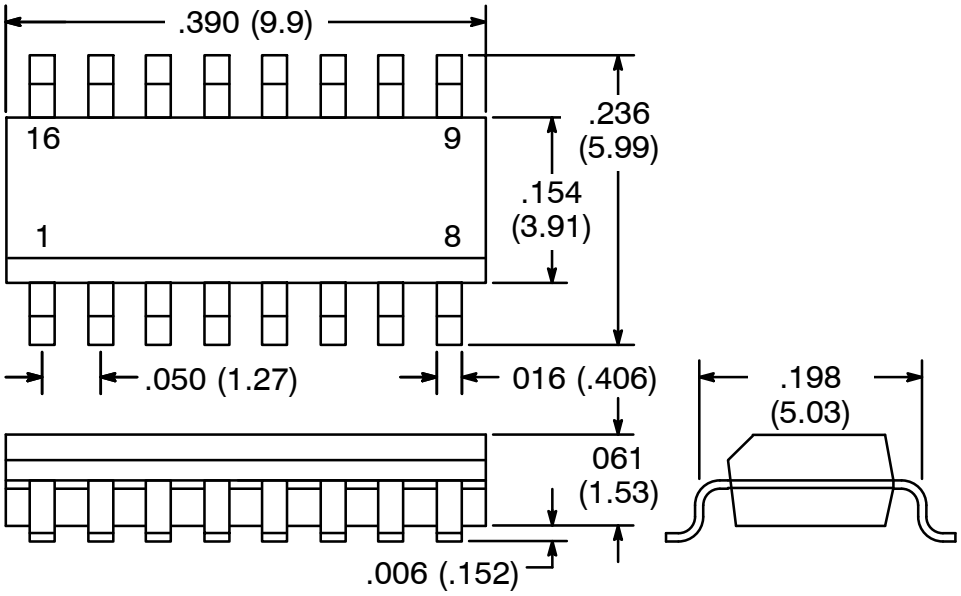
Pin Connection Diagram



NTE4020B



NTE4020BT



NOTE: Pin1 on Beveled Edge