NTE4021B & NTE4021BT
Integrated Circuit
CMOS, 8−Bit Static Shift Register

Description:

The NTE4021B (16−Lead DIP) and NTE4021BT (SOIC−16) are 8−bit static shift registers constructed with MOS P−Channel and N−Channel enhancement mode devices in a single monolithic structure. The These devices find primary use in parallel−to−serial data conversion, asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

Features:

- Asynchronous Parallel Input/Serial Output
- Synchronous Serial Output/Serial Output
- Full Static Operation
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Double Diode Input Protection
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . −0.5 to +18.0V

Input Voltage (DC or Transient), V_{in} . . . . −0.5 to V_{DD} to +0.5V

Output Voltage (DC or Transient), V_{out} . . . . −0.5 to V_{DD} to +0.5V

Input Current (DC or Transient, Per Pin), I_{in} . . . . ±10mA

Output Current (DC or Transient, Per Pin), I_{out} . . . . ±10mA

Power Dissipation (Per Package), P_D 500mW

       Temperature Derating (from +65° to +125°C) . . . . −7.0mW/°C

Storage Temperature, T_{stg} . . . . −65° to +150°C

Lead Temperature (During Soldering, 8sec max), T_L . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V$_{SS}$, Note 2)

Parameter		Symbol	V$_{DD}$ Vdc	−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit
Output Voltage "0" Level		V$_{OL}$	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V$_{in}$ = V$_{DD}$ or 0			10	–	0.05	–	0	0.05	–	0.05	Vdc
			15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level		V$_{OH}$	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V$_{in}$ = 0 or V$_{DD}$			10	9.95	–	9.95	10	–	9.95	–	Vdc
			15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level (V$_O$ = 4.5 or 0.5Vdc)		V$_{IL}$	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V$_O$ = 9.0 or 1.0Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V$_O$ = 13.5 or 1.5Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level (V$_O$ = 0.5 or 4.5Vdc)		V$_{IH}$	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V$_O$ = 1.0 or 9.0Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V$_O$ = 1.5 or 13.5Vdc)			15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source (V$_{OH}$ = 2.5Vdc)		I$_{OH}$	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V$_{OH}$ = 4.6Vdc)			5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V$_{OH}$ = 9.5Vdc)			10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V$_{OH}$ = 13.5Vdc)			15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Sink (V$_{OL}$ = 0.4Vdc)		I$_{OL}$	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V$_{OL}$ = 0.5Vdc)			10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V$_{OL}$ = 1.5Vdc)			15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current		I$_{in}$	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V$_{IN}$ = 0)		C$_{in}$	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)		I$_{DD}$	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
			10	–	10	–	0.010	10	–	300	µAdc
			15	–	15	–	0.015	15	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C$_L$ = 50pF on All Buffers Switching Note 3, Note 4)		I$_T$	5.0	I$_T$ = (0.75µA/kHz) f + I$_{DD}$							µAdc
			10	I$_T$ = (1.5µA/kHz) f + I$_{DD}$							µAdc
			15	I$_T$ = (2.25µA/kHz) f + I$_{DD}$							µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50) V_{fk}$$

where: I$_T$ is in µA (per package), C$_L$ in pF, V = (V$_{DD}$ − V$_{SS}$) in volts, f in kHz is input frequency, and k = 0.0015.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5ns/pf) C_L + 25ns	t_{TLH}, t_{THL}	5.0	–	100	200	ns
t_{TLH}, t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{TLH}, t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time (Clock to Q, P/S to Q) t_{PHL}, t_{PLH} = (1.7ns/pf) C_L + 315ns	t_{PLH}, t_{PHL}	5.0	–	400	800	ns
t_{PHL}, t_{PLH} = (0.66ns/pf) C_L + 137ns		10	–	170	340	ns
t_{PHL}, t_{PLH} = (0.5ns/pf) C_L + 90ns		15	–	115	230	ns
Clock Pulse Width	t_{WH}	5.0	400	150	–	ns
		10	175	75	–	ns
		15	135	40	–	ns
Clock Frequency	f_{cl}	5.0	–	3.0	1.5	MHz
		10	–	6.0	3.0	MHz
		15	–	8.0	4.0	MHz
Parallel/Serial Control Pulse Width	t_{WH}	5.0	400	150	–	ns
		10	175	75	–	ns
		15	135	40	–	ns
Setup Time, P/S to Clock	t_{su}	5.0	200	100	–	ns
		10	100	50	–	ns
		15	80	40	–	ns
Hold Time, P/S to Clock	t_h	5.0	20	–2.5	–	ns
		10	20	–10	–	ns
		15	25	0	–	ns
Setup Time, Data (Parallel or Serial) to Clock or P/S	t_{su}	5.0	350	150	–	ns
		10	80	50	–	ns
		15	60	30	–	ns
Hold Time, Clock to D_S	t_h	5.0	45	0	–	ns
		10	35	0	–	ns
		15	35	5	–	ns
Hold Time, Clock to P_n	t_h	5.0	50	25	–	ns
		10	45	20	–	ns
		15	45	20	–	ns
Input Clock Rise Time	$T_{r(cl)}$	5.0	–	–	15	ns
		10	–	–	5	ns
		15	–	–	4	ns

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.
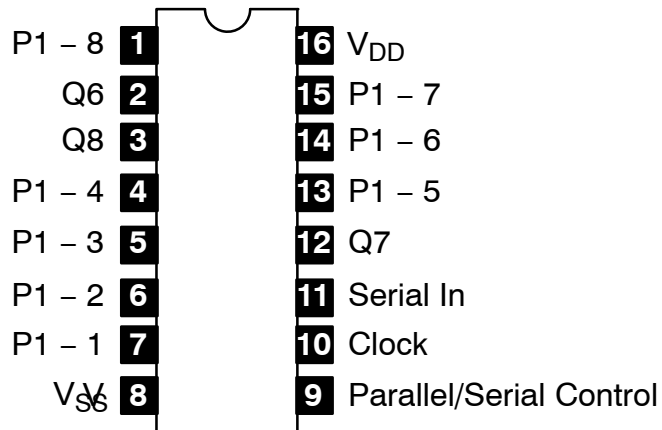
Truth Table:

Serial Operation

t	Clock	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n	_/‾	0	0	0	?	?
n+1	_/‾	1	0	1	0	?
n+2	_/‾	0	0	0	1	0
n+3	_/‾	1	0	1	0	1
	‾_	X	0	Q6	Q7	Q8

Parallel Operation

Clock	D_S	P/S	P_n	*Q_n
_/‾	X	X	0	0
_/‾	X	X	1	1

* = Q6, Q7, & Q8 are available externally
X = Don't Care

Pin Connection Diagram

P1 – 8	1	16	V_{DD}
Q6	2	15	P1 – 7
Q8	3	14	P1 – 6
P1 – 4	4	13	P1 – 5
P1 – 3	5	12	Q7
P1 – 2	6	11	Serial In
P1 – 1	7	10	Clock
V_{SS}	8	9	Parallel/Serial Control

NTE4021B

16   9

1   8

.870 (22.0) Max

.260 (6.6)
Max

.200 (5.08)
Max

.100 (2.54)

.099 (2.5) Min

.700 (17.78)

NTE4021BT

.390 (9.9)

16   9

1   8

.236
(5.99)

.154
(3.91)

.050 (1.27)   016 (.406)

.198
(5.03)

061
(1.53)

.006 (.152)
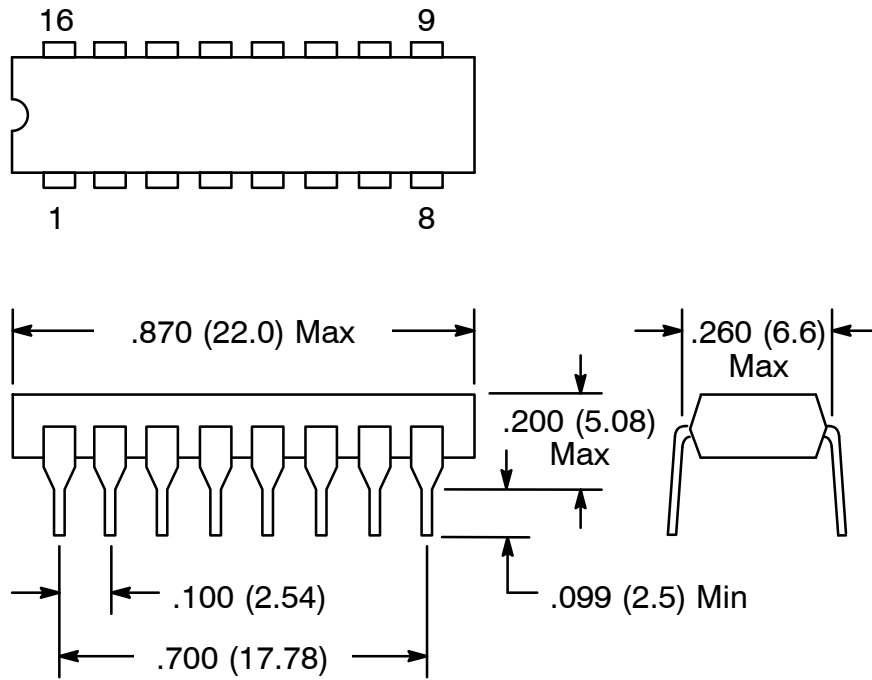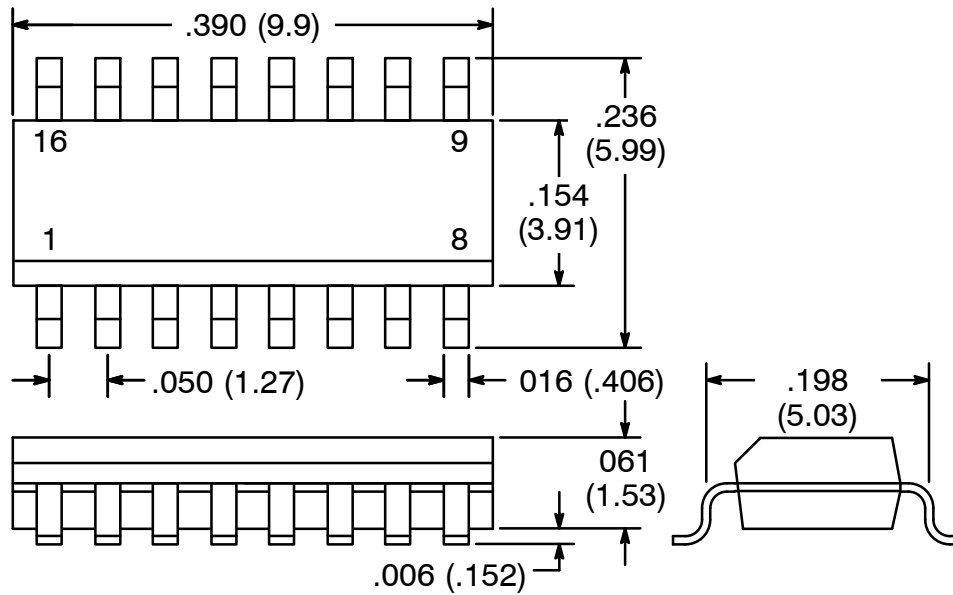
NOTE: Pin1 on Beveled Edge