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NTE4583B
Integrated Circuit
CMOS – Dual Schmitt Trigger

Description:

The NTE4583B is a dual Schmitt trigger constructed with complementary P–channel and N–channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3–state input and an internally–connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed–up of a slow waveform edge in interface receivers, level detectors, etc.

Features:

- Diode Protection on All Inputs
- Supply Voltage Range: 3V to 18V
- Single Supply Operation
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Resistor Adjustable Trigger Levels

Absolute Maximum Ratings: (Voltages Referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input or Output Voltage (DC or Transient), V_{in}, V_{out} . . . . . –0.5 to V_{DD}+0.5V
Input or Output Current, per Pin (DC or Transient), I_{in}, I_{out} . . . . . ±10mA
Power Dissipation, per Package, P_D 500mW
Derate Above +65°C . . . . . 12mW/°C
Operating Temperature Range, T_{opr} . . . . . –40° to +85°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec), T_L . . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Note 2. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

Electrical Characteristics: (Voltages Referenced to V_{SS}, Note 3)

Parameter	Symbol	V_{DD}	−40°C		+25°C			+85°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output "0" Level Voltage V_{in} = V_{DD} or 0	V_{OL}	5	–	0.05	–	0	0.05	–	0.05	V
		10	–	0.05	–	0	0.05	–	0.05	V
		15	–	0.05	–	0	0.05	–	0.05	V
Output "1" Level Voltage V_{in} = 0 or V_{DD}	V_{OH}	5	4.95	–	4.95	5	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	V
		15	14.95	–	14.95	15	–	14.95	–	V
Input "0" Level Voltage, A and B V_O = 4.5V or 0.5V	V_{IL}	5	–	1.5	–	2.25	1.5	–	1.5	V
V_O = 9.0V or 1.0V		10	–	3.0	–	4.50	3.0	–	3.0	V
V_O = 13.5V or 1.5V		15	–	4.0	–	6.75	4.0	–	4.0	V
Input "1" Level Voltage, A and B V_O = 0.5V or 4.5V	V_{IH}	5	3.5	–	3.5	2.75	–	3.5	–	V
V_O = 1.0V or 9.0V		10	7.0	–	7.0	5.50	–	7.0	–	V
V_O = 1.5V or 13.5V		15	11.0	–	11.0	8.25	–	11.0	–	V
Output Drive Source Current V_{OH} = 2.5V	I_{OH}	5	–1.0	–	–0.8	–1.7	–	–0.6	–	mA
V_{OH} = 4.6V		5	–0.2	–	–0.16	–0.36	–	–0.12	–	mA
V_{OH} = 9.5V		10	–0.5	–	–0.4	–0.9	–	–0.3	–	mA
V_{OH} = 13.5V		15	–1.4	–	–1.2	–3.5	–	–1.0	–	mA
Output Drive Sink Current V_{OL} = 0.4V	I_{OL}	5	0.52	–	0.44	0.88	–	0.36	–	mA
V_{OL} = 0.5V		10	1.3	–	1.1	2.25	–	0.9	–	mA
V_{OL} = 1.5V		15	3.6	–	3.0	8.8	–	2.4	–	mA
Input Current	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Input Capacitance, V_{in} = 0	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current, Per Package	I_{DD}	5	–	1.0	–	0.0005	1.0	–	7.5	μA
		10	–	2.0	–	0.0010	2.0	–	15.0	μA
		15	–	4.0	–	0.0015	4.0	–	30.0	μA
Total Supply Current Dynamic plus Quiescent, Per Package C_L = 50pF on all outputs, all buffers switching (Note 4)	I_T	5	I_T = (1.33μA/kHz) f + I_{DD}							μA
		10	I_T = (2.65μA/kHz) f + I_{DD}							μA
		15	I_T = (3.98μA/kHz) f + I_{DD}							μA
Three−State Leakage Current	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	μA

Note 3. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

Note 4. The formulas given are for the typical characteristics only at +25°C. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA, C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 3, Note 5)

Parameter	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time t_{TLH} = (3.0ns/pF) C_L + 30ns	t_{TLH}	5	–	180	360	ns
t_{TLH} = (1.5ns/pF) C_L +15ns		10	–	90	180	ns
t_{TLH} = (1.1ns/pF) C_L + 10ns		15	–	65	130	ns
Output Fall Time t_{THL} = (1.5ns/pF) C_L + 25ns	t_{THL}	5	–	100	200	ns
t_{THL} = (0.75ns/Pf) C_L + 12.5ns		10	–	50	100	ns
t_{THL} = (0.55ns/pF) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time, A_{in}, B_{in} to A_{out}, B_{out} t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 565ns	t_{PLH}, t_{PHL}	5	–	650	1300	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 197ns		10	–	230	460	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 125ns		15	–	150	300	ns
Propagation Delay Time, A_{in}, B_{in} to A_{out}, B_{out} t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 1015ns	t_{PLH}, t_{PHL}	5	–	1100	2200	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 347ns		10	–	380	760	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 235ns		15	–	260	520	ns
Propagation Delay Time, A_{in}, B_{in} to Exclusive OR t_{PLH}, t_{PHL} = (1.7ns/pF) C_L + 665ns	t_{PLH}, t_{PHL}	5	–	750	1500	ns
t_{PLH}, t_{PHL} = (0.66ns/pF) C_L + 257ns		10	–	280	560	ns
t_{PLH}, t_{PHL} = (0.5ns/pF) C_L + 145ns		15	–	170	340	ns
3–State Enable, Disable Delay Time t_{on}, t_{off} = (1.7ns/pF) C_L + 140ns	t_{on}, t_{off}	5	–	225	450	ns
t_{on}, t_{off} = (0.66ns/pF) C_L + 57ns		10	–	90	180	ns
t_{on}, t_{off} = (0.5ns/pF) C_L + 30ns		15	–	55	110	ns
Positive Threshold Voltage R1, R2 = 5.0kΩ	V_{T+}	5	–	3.30	–	V
		10	–	5.70	–	V
		15	–	8.20	–	V
Negative Threshold Voltage R1, R2 = 5.0kΩ	V_{T-}	5	–	1.70	–	V
		10	–	4.30	–	V
		15	–	6.80	–	V
Hysteresis Voltage R1, R2 = 5.0kΩ	V_H	5	0.85	1.70	3.40	V
		10	0.70	1.40	2.80	V
		15	0.70	1.40	2.80	V
Threshold Voltage Variation, A to B R1, R2 = 5.0kΩ	ΔV_T	5	–	1.10	–	V
		10	–	0.15	–	V
		15	–	0.20	–	V

Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

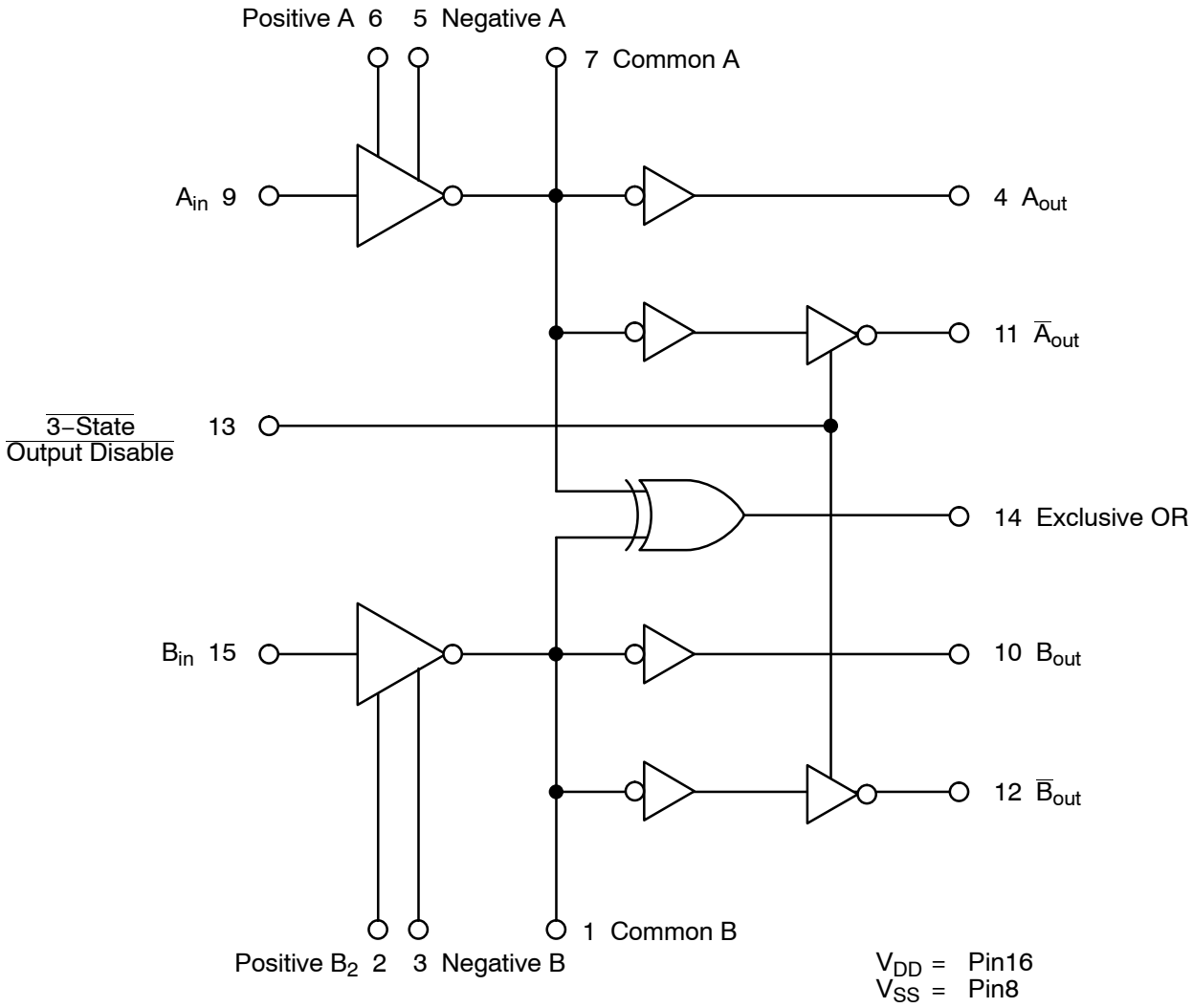
Note 5. The formulas given are for the typical characteristics only at +25°C.

Truth Table

Inputs			Outputs				
A	**B**	**$\overline{Dis}$**	**A_{out}**	**$\overline{A}_{out}$**	**B_{out}**	**$\overline{B}_{out}$**	**Exclusive OR**
0	0	0	0	Z	0	Z	0
0	0	1	0	1	0	1	0
0	1	0	0	Z	1	Z	1
0	1	1	0	1	1	0	1
1	0	0	1	Z	0	Z	1
1	0	1	1	0	0	1	1
1	1	0	1	Z	1	Z	0
1	1	1	1	0	1	0	0

Z = High impedance at output

Logic Diagram



Pin Connection Diagram