



ELECTRONICS, INC.  
 44 FARRAND STREET  
 BLOOMFIELD, NJ 07003  
 (973) 748-5089  
<http://www.nteinc.com>

## NTE7096-1 Integrated Circuit High Performance Mode Pulse Width Modulator (PWM) Controller 8-Lead DIP Type Package

**Description:**

The NTE7096-1 is a high performance pulse width modulator controller in an 8-Lead DIP type package that provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include a trimmed oscillator for precise DUTY CYCLE CONTROL, under voltage lockout featuring start-up current less than 0.5mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off-state.

The NTE7096-1 has a UVLO threshold of 16V (on) and 10V (off), ideally suited for off-line applications and can operate to duty cycles approaching 100%.

**Features:**

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250kHz
- Current Mode Operation to 500kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-by-Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Start-Up and Operating Current

**Absolute Maximum Ratings:**

Supply Voltage (Low Impedance Source), $V_I$ .....	30V
Supply Voltage ( $I_i < 30mA$ ), $V_I$ .....	Self Limiting
Output Current, $I_O$ .....	$\pm 1A$
Output Energy (Capacitive Load), $E_O$ .....	5 $\mu$ J
Analog Inputs (Pin2, Pin3) .....	-0.3 to 5.5V
Error Amplifier Output Sink Current .....	10mA
Power Dissipation ( $T_A \leq +25^\circ C$ ), $P_{tot}$ .....	1.25W
Operating Junction Temperature Range, $T_J$ .....	-40° to +150°C
Storage Temperature Range, $T_{stg}$ .....	-65° to +150°C
Maximum Thermal Resistance, Junction-to-Ambient, $R_{thJA}$ .....	+100°C/W
Lead Temperature (During Soldering, 10sec), $T_L$ .....	+300°C

Note 1. All voltages are with respect to Pin5, all currents are positive into the specified terminal.



**Electrical Characteristics:** (Note 2,  $0^{\circ} \leq T_A \leq +70^{\circ}\text{C}$ ,  $V_I = 15\text{V}$  (Note 6),  $R_T = 10\text{K}$ ,  $C_T = 3.3\text{nF}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Reference Section</b>						
Output Voltage	$V_{\text{REF}}$	$T_J = +125^{\circ}\text{C}$ , $I_O = 1\text{mA}$	4.9	5.0	5.1	V
Line Regulation	$\Delta V_{\text{REF}}$	$12\text{V} \leq V_I \leq 25\text{V}$	–	2	20	mV
Load Regulation	$\Delta V_{\text{REF}}$	$1\text{mA} \leq I_O \leq 20\text{mA}$	–	3	25	mV
Temperature Stability	$\Delta V_{\text{REF}}/\Delta T$	Note 3	–	0.2	–	mV/ $^{\circ}\text{C}$
Total Output Variation		Line, Load, Temperature	4.82	–	5.18	V
Output Noise Voltage	$e_N$	$10\text{Hz} \leq f \leq 10\text{kHz}$ , $T_J = +25^{\circ}\text{C}$ , Note 3	–	50	–	$\mu\text{V}$
Long Term Stability		$T_A = +125^{\circ}\text{C}$ , 1000 Hrs, Note 3	–	5	25	mV
Output Short Circuit	$I_{\text{SC}}$		–30	–100	–180	mA
<b>Oscillator Section</b>						
Frequency	$f_{\text{OSC}}$	$T_J = +25^{\circ}\text{C}$	49	52	55	kHz
		$T_A = T_{\text{low}}$ to $T_{\text{high}}$	48	–	56	kHz
		$T_J = +25^{\circ}\text{C}$ ( $R_T = 6.2\text{k}$ , $C_T = 1\text{nF}$ )	225	250	275	kHz
Frequency Change with Vltg	$\Delta f_{\text{OSC}}/\Delta V$	$V_{\text{CC}} = 12\text{V}$ to $25\text{V}$	–	0.2	1	%
Frequency Change with Temp	$\Delta f_{\text{OSC}}/\Delta T$	$T_A = T_{\text{low}}$ to $T_{\text{high}}$	–	0.5	–	%
Oscillator Voltage Swing	$V_{\text{OSC}}$	(Peak-to-Peak)	–	1.6	–	V
Discharge Current ( $V_{\text{OSC}} = 2\text{V}$ )	$I_{\text{dischg}}$	$T_J = +25^{\circ}\text{C}$	7.8	8.3	8.8	mA
		$T_A = T_{\text{low}}$ to $T_{\text{high}}$	7.6	–	8.8	mA
<b>Error Amp Section</b>						
Input Voltage	$V_2$	$V_{\text{PIN1}} = 2.5\text{V}$	2.42	2.50	2.58	V
Input Bias Current	$I_b$	$V_{\text{FB}} = 5\text{V}$	–	–0.1	–2.0	$\mu\text{A}$
$A_{\text{VOL}}$		$2\text{V} \leq V_O \leq 4\text{V}$	65	90	–	dB
Utility Gain Bandwidth	BW	$T_J = +25^{\circ}\text{C}$	0.7	1.0	–	MHz
Power Supply Rejection Ratio	PSRR	$12\text{V} \leq V_I \leq 25\text{V}$	60	70	–	dB
Output Sink Current	$I_O$	$V_{\text{PIN2}} = 2.7\text{V}$ , $V_{\text{PIN1}} = 1.1\text{V}$	2	12	–	mA
Output Source Current	$I_O$	$V_{\text{PIN2}} = 2.3\text{V}$ , $V_{\text{PIN1}} = 5\text{V}$	–0.5	–1.0	–	mA
$V_{\text{OUT High}}$		$V_{\text{PIN2}} = 2.3\text{V}$ , $R_L = 15\text{k}\Omega$ to GND	5.0	6.2	–	V
$V_{\text{OUT Low}}$		$V_{\text{PIN2}} = 2.7\text{V}$ , $R_L = 15\text{k}\Omega$ to Pin8	–	0.8	1.1	V
<b>Current Sense Section</b>						
Gain	$G_V$	Note 4, Note 5	2.85	3.00	3.15	V/V
Maximum Input Signal	$V_3$	$V_{\text{PIN1}} = 5\text{V}$ , Note 4	0.9	1.0	1.1	V
Supply Voltage Rejection	SVR	$12\text{V} \leq V_I \leq 25\text{V}$ , Note 4	–	70	–	dB
Input Bias Current	$I_b$		–	–2	–10	$\mu\text{A}$
Delay to Output			–	150	300	ns

Note 2. Max. package power dissipation limits must be respected; low duty cycle pulse techniques are used during test. Maintain  $T_J$  as close to  $T_A$  as possible.

Note 3. These parameters, although guaranteed, are not 100% tested in production.

Note 4. Parameter measured at trip point of latch with  $V_{\text{PIN2}} = 0$ .

Note 5. Gain defined as:  $A = \Delta V_{\text{PIN1}} / \Delta V_{\text{PIN3}}$ ;  $0 \leq V_{\text{PIN3}} \leq 0.8\text{V}$ .

Note 6. Adjust  $V_I$  above the start threshold before setting at 15V.

**Electrical Characteristics (Cont'd):** (Note 2,  $0^{\circ} \leq T_A \leq +70^{\circ}\text{C}$ ,  $V_I = 15\text{V}$  (Note 6),  $R_T = 10\text{K}$ ,  $C_T = 3.3\text{nF}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Output Section</b>						
Output Low Level	$V_{OL}$	$I_{SINK} = 20\text{mA}$	-	0.1	0.4	V
		$I_{SINK} = 200\text{mA}$	-	1.6	2.2	V
Output High Level	$V_{OH}$	$I_{SOURCE} = 20\text{mA}$	13.0	13.5	-	V
		$I_{SOURCE} = 200\text{mA}$	12.0	13.5	-	V
UVLO Saturation	$V_{OLS}$	$V_{CC} = 6\text{V}$ , $I_{SINK} = 1\text{mA}$	-	0.1	1.1	V
Rise Time	$t_r$	$T_J = +25^{\circ}\text{C}$ , $C_L = 1\text{nF}$ , Note 3	-	50	150	ns
Fall Time	$t_f$		-	50	150	ns
<b>Undervoltage Lockout Section</b>						
Start Threshold			14.5	16.0	17.5	V
Min. Operating Voltage after Turn-On			8.5	10.0	11.5	V
<b>PWM Section</b>						
Maximum Duty Cycle			94	96	100	%
Minimum Duty Cycle			-	-	0	%
<b>Total Standby Current</b>						
Start-Up Current	$I_{st}$	$V_I = 14\text{V}$	-	0.3	0.5	mA
Operating Supply Current	$I_I$	$V_{PIN2} = V_{PIN3} = 0\text{V}$	-	12	17	mA
Zener Voltage	$V_{iz}$	$I_I = 258\text{mA}$	30	36	-	V

Note 2. Max. package power dissipation limits must be respected; low duty cycle pulse techniques are used during test. Maintain  $T_J$  as close to  $T_A$  as possible.

Note 3. These parameters, although guaranteed, are not 100% tested in production.

Note 4. Parameter measured at trip point of latch with  $V_{PIN2} = 0$ .

Note 5. Gain defined as:  $A = \Delta V_{PIN1} / \Delta V_{PIN3}$ ;  $0 \leq V_{PIN3} \leq 0.8\text{V}$ .

Note 6. Adjust  $V_I$  above the start threshold before setting at 15V.

**Pin Connection Diagram**



