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NTE7485
Integrated Circuit
TTL – 4–Bit Magnitude Comparator

Description:

The NTE7485 is a 4–bit magnitude comparator in a 16–Lead plastic DIP type package that performs comparison of straight binary and straight BCD (8–4–2–1) codes. Three fully decoded decisions about two 4–bit words (A, B) are made and are externally available at three outputs. This device is fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less–significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more–significant bits. The stage handling the least–significant bits must have low–level voltages applied to the A > B and A < B inputs. The cascading paths are implemented with only a two–gate–level delay to reduce overall comparison times for long words.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
Input Voltage, V_{IN} 5.5V
Interemitter Voltage (Note 2) 5.5V
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Voltage values, except interemitter voltages, are with respect to network ground terminal.
Note 2. This is the voltage between two emitters of a multiple–emitter input transistor. This rating applies to each A input in conjunction with its respective B input.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Output Current	I_{OH}	–	–	–400	μA
Low–Level Output Current	I_{OL}	–	–	16	mA
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 3, Note 4)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2	–	–	V
Low Level Input Voltage	V_{IL}		–	–	0.7	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −400μA	2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 4mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current A < B, A > B Inputs	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	40	μA
All Other Inputs			–	–	120	μA
Low Level Input Current A < B, A > B Inputs	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	−1.6	mA
All Other Inputs			–	–	−4.8	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, V_O = 0, Note 5	−18	–	−55	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 6	–	55	88	mA

Note 3. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 4. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 5. Not more than one output should be shorted at a time.

Note 6. I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5V.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

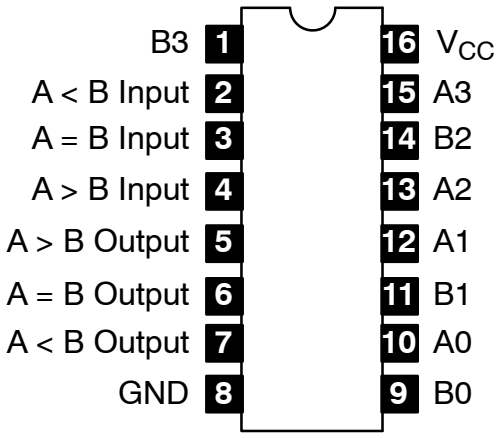
Parameter	Symbol	From Input	To Output	Number of Gate Levels	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time	t_{PLH}	Any A or B Data Input	A < B, A > B	1	R_L = 400Ω, C_L = 15pF	–	7	–	ns
				2		–	12	–	ns
				3		–	17	26	ns
			A = B	4		–	23	35	ns
Propagation Delay Time	t_{PHL}	Any A or B Data Input	A < B, A > B	1		–	11	–	ns
				2		–	15	–	ns
				3		–	20	30	ns
			A = B	4		–	20	30	ns
Propagation Delay Time	t_{PLH}	A < B or A = B	A > B	1		–	7	11	ns
Propagation Delay Time	t_{PHL}	A < B or A = B	A > B	1		–	11	17	ns
Propagation Delay Time	t_{PLH}	A = B	A = B	2		–	13	20	ns
Propagation Delay Time	t_{PHL}	A = B	A = B	2		–	11	17	ns
Propagation Delay Time	t_{PLH}	A > B or A = B	A < B	1		–	7	11	ns
Propagation Delay Time	t_{PHL}	A > B or A = B	A < B	1		–	11	17	ns

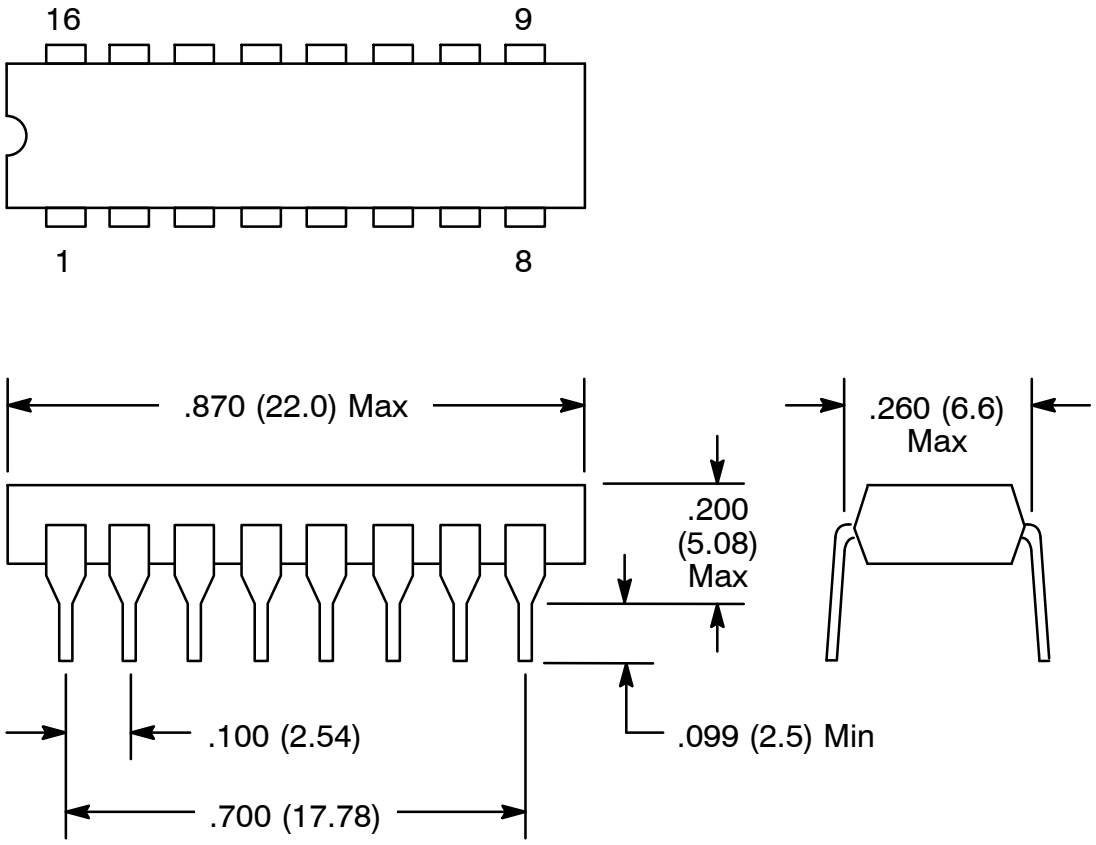
Function Table:

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**A > B**	**A < B**	**A = B**	**A > B**	**A < B**	**A = B**
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A2 < B2	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A2 = B2	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A2 = B2	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A2 = B2	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A2 = B2	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A2 = B2	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A2 = B2	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A2 = B2	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A2 = B2	A0 = B0	L	L	L	H	H	L

H = HIGH Level
L = LOW Level
X = Irrelevant

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)