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NTE74HC245
Integrated Circuit
TTL – High Speed CMOS,
Octal Bus Transceiver with 3–State
Non–Inverting Outputs

Description:

The NTE74HC245 is a high–speed octal 3–state bidirectional transceiver in a 20–Lead DIP type package intended for two–way asynchronous communication between data buses. It contains high drive current outputs which enable high–speed operation while driving large bus capacitances. It also provides the low power consumption of standard CMOS circuits with speeds and drive capabilities comparable to that of LS–TTL circuits.

The NTE74HC245 allows data transmission of the B bus or from the B bus to the A bus. The logic level at the direction input (DIR) determines the direction. The output enable input ($\overline{OE}$), when high, puts the I/O ports in the high impedance state.

Features:

- Wide Power Supply Range: 2V to 6V
- High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- 3–State Outputs
- Buffered Inputs
- Bus Line Driving Capability
- High–Current Bus Driver Outputs
- Fanout (Over Temperature Range):
  - Standard Outputs . . . 10 LS–TTL Loads
  - Bus Driver Outputs . . 15 LS–TTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LS–TTL Logic ICs

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Drain Current (Per Output), I_{OUT} . . . . . ±35mA
DC Output Source or Sink Current (Per Output), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Maximum Junction, T_J . . . . . +150°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Typical Thermal Resistance, Junction–to–Ambient, R_{thJA} . . . . . 125°C/W
Lead Temperature (During Soldering, 10sec), T_L . . . . . +300°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.0	–	6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C
Input Rise or Fall Times	t_r, t_f				
V_{CC} = 2.0V		–	–	1000	ns
V_{CC} = 4.5V		–	–	500	ns
V_{CC} = 6.0V		–	–	400	ns

DC Electrical Characteristics:

Parameter	Symbol	Test Conditions		V_{CC}	T_A = +25°C	T_A = –40° to +85°C		Unit
					Typ	Guaranteed Limits		
Minimum HIGH Level Input Voltage	V_{IH}			2.0	–	1.5	1.5	V
				4.5	–	3.15	3.15	V
				6.0	–	4.2	4.2	V
Maximum LOW Level Input Voltage	V_{IL}			2.0	–	0.5	0.5	V
				4.5	–	1.35	1.35	V
				6.0	–	1.8	1.8	V
Minimum HIGH Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OUT} = –20μA	–	V_{CC}	V_{CC} –0.1	V_{CC} –0.1	V
			I_{OUT} = –4mA	4.5	–	3.98	3.84	V
			I_{OUT} = –5.2mA	6.0	–	5.48	5.34	V
Minimum LOW Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OUT} = 20μA	–	–	0.1	0.1	V
			I_{OUT} = 4mA	4.5	–	0.26	0.33	V
			I_{OUT} = 5.2mA	6.0	0–	0.26	0.33	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	±0.1	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		6.0	–	8.0	80	μA
3–State Leakage Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}		6.0	–	±0.5	±0.5	μA

AC Electrical Characteristics: (t_r = t_f = 6ns, C_L = 50pF unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC}	T_A = +25°C	T_A = –40° to +85°C		Unit
				Typ	Guaranteed Limits		
Propagation Delay (Data to Outputs)	t_{PHL}, t_{PLH}		2.0	–	110	140	ns
			4.5	–	22	28	ns
		C_L = 15pF	5.0	9	–	–	ns
			6.0	–	19	24	ns
Propagation Delay (Output Disable to Outputs)	t_{PHL}, t_{PLH}		2.0	–	150	190	ns
			4.5	–	30	38	ns
		C_L = 15pF	5.0	12	–	–	ns
			6.0	–	26	33	ns
Propagation Delay (Output Enable to Outputs)	t_{PHL}, t_{PLH}		2.0	–	150	190	ns
			4.5	–	30	38	ns
		C_L = 15pF	5.0	12	–	–	ns
			6.0	–	26	33	ns

AC Electrical Characteristics (Cont'd): ($t_r = t_f = 6ns$, $C_L = 50pF$ unless otherwise specified)

Parameter	Symbol	Test Conditions	V_{CC}	$T_A = +25°C$	$T_A = -40°$ to $+85°C$		Unit
				Typ	Guaranteed Limits		
Output Transition Time	t_{THL}, t_{TLH}		2.0	–	60	75	ns
			4.5	–	12	15	ns
			6.0	–	10	13	ns
Maximum Input Capacitance	C_{IN}		–	–	10	10	pF
Maximum 3−State Output Capacitance	C_{OUT}		–	–	20	20	pF
Power Dissipation Capacitance	C_{PD}	Note 3	5	53	–	–	pF

Note 3. C_{PD} is used to determine the dynamic power consumption, per channel.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, f_O = Output Frequency,
C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

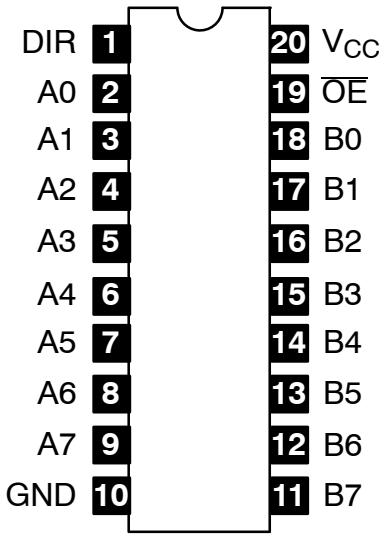
Truth Table:

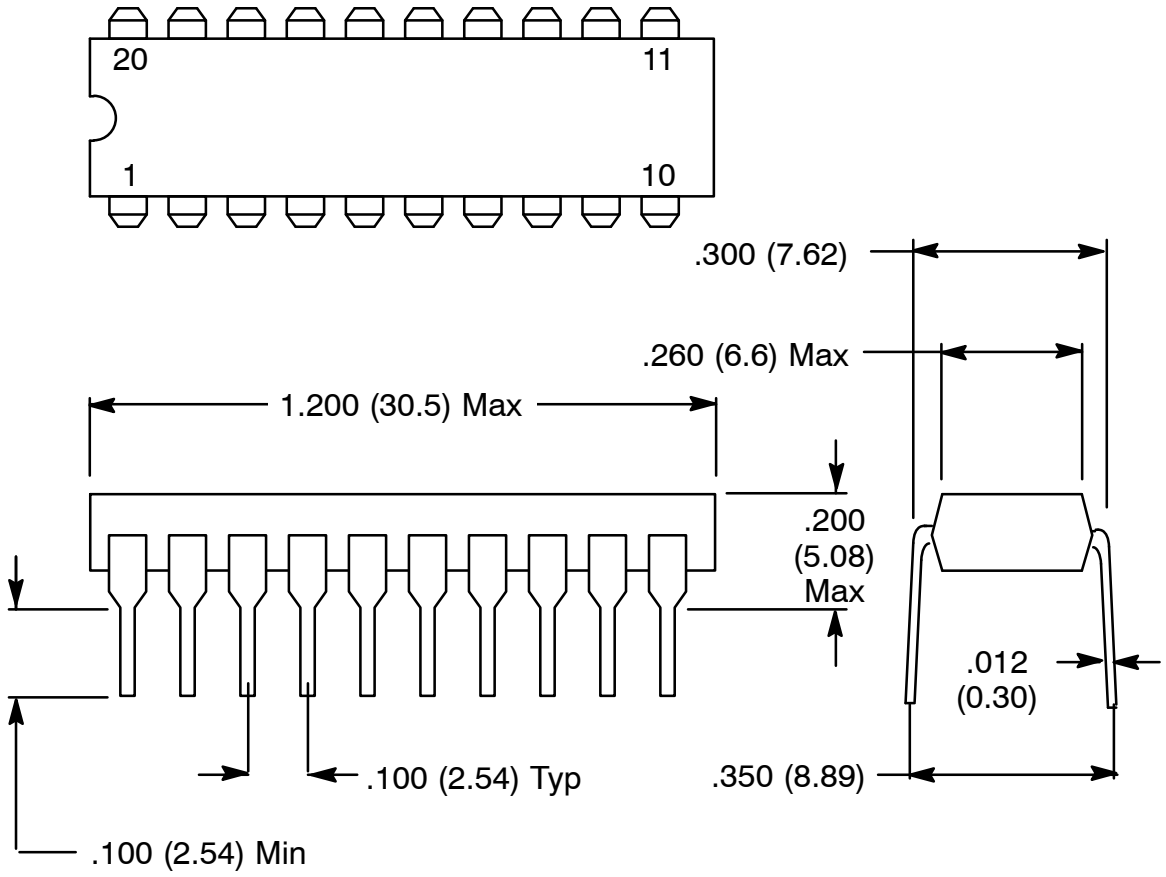
Control Inputs		Operation
$\overline{OE}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

H = HIGH Level
L = LOW Level
X = Irrelevant

To prevent excess currents in the High−Z (Isolation) modes all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

Pin Connection Diagram




20
11
1
10
.300 (7.62)
.260 (6.6) Max
1.200 (30.5) Max
.200
(5.08)
Max
.012
(0.30)
.100 (2.54) Typ
.350 (8.89)
.100 (2.54) Min