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## NTE74HCT273 Integrated Circuit TTL – High Speed CMOS, Octal D–Type Flip–Flop with Clear

**Description:**

The NTE74HCT273 is a positive edge–triggered flip–flop in a 20–Lead DIP type package that has a common clock and clear–independent Q outputs. Data on a D input, having the specified set–up and hold time, is transferred to the corresponding Q output on the positive–going transition of the clock pulse. The asynchronous clear forces all outputs low when it is low.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to  $V_{CC}$  and GND.

**Features:**

- Typical Propagation Delay: 20ns
- Low Quiescent Current: 80 $\mu$ A (max)
- Fanout of 10 LS–TTL Loads

**Absolute Maximum Ratings:** (Note 1, Note 2)

Supply Voltage, $V_{CC}$ .....	–0.5 to +7.0V
DC Input Voltage, $V_{IN}$ .....	–1.5 to $V_{CC} + 1.5V$
DC Output Voltage, $V_{OUT}$ .....	–0.5 to $V_{CC} + 0.5V$
Clamp Diode Current, $I_{IK}, I_{OK}$ .....	$\pm 20mA$
DC Output Current (Per Pin), $I_{OUT}$ .....	$\pm 25mA$
DC $V_{CC}$ or GND Current (Per Pin), $I_{CC}$ .....	$\pm 50mA$
Power Dissipation (Note 3), $P_D$ .....	500mW
Storage Temperature Range, $T_{stg}$ .....	–65°C to +150°C
Lead Temperature (During Soldering, 10sec), $T_L$ .....	+260°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2. Unless otherwise specified, all voltages are referenced to GND.

Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

**Recommended Operating Conditions:**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.5	–	5.5	V
DC Input or Output Voltage	$V_{IN}, V_{OUT}$	0	–	$V_{CC}$	V
Operating Temperature Range	$T_A$	–40	–	+85	°C
Input Rise or Fall Times	$t_r, t_f$	–	–	500	ns

**DC Electrical Characteristics:** ( $V_{CC} = 5V \pm 10\%$  unless otherwise specified)

Parameter	Symbol	Test Conditions	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ \text{ to } +85^\circ\text{C}$		Unit
			Typ	Guaranteed Limits			
Minimum High Level Input Voltage	$V_{IH}$		–	2.0	2.0		V
Maximum Low Level Input Voltage	$V_{IL}$		–	0.8	0.8		V
Minimum High Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$ I_{OUT}  = 20\mu\text{A}$	$V_{CC}$	$V_{CC}^{-0.1}$	$V_{CC}^{-0.1}$	V
			$ I_{OUT}  = 4.0\text{mA}, V_{CC} = 4.5\text{V}$	4.2	3.98	3.84	V
			$ I_{OUT}  = 4.8\text{mA}, V_{CC} = 5.5\text{V}$	5.7	4.98	4.84	V
Maximum Low Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$	$ I_{OUT}  = 20\mu\text{A}$	0	0.1	0.1	V
			$ I_{OUT}  = 4.0\text{mA}, V_{CC} = 4.5\text{V}$	0.2	0.26	0.33	V
			$ I_{OUT}  = 4.8\text{mA}, V_{CC} = 5.5\text{V}$	0.2	0.26	0.33	V
Maximum Input Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND, $V_{IH}$ or $V_{IL}$	–	$\pm 0.1$	$\pm 1.0$		$\mu\text{A}$
Maximum Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu\text{A}$	–	8	80		$\mu\text{A}$
		$V_{IN} = 2.4\text{V}$ or $0.5\text{V}$ , Note 4	–	0.6	0.8		$\mu\text{A}$

Note 4. This is measured per input with all other inputs held at  $V_{CC}$  or GND.

**AC Electrical Characteristics:** ( $V_{CC} = 5V$ ,  $t_r = t_f = 6\text{ns}$ ,  $C_L = 15\text{pF}$ ,  $T_A = +25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits		Unit
Maximum Operating Frequency	$f_{MAX}$		68	30		MHz
Maximum Propagation Delay (Clock to Q)	$t_{PHL}, t_{PLH}$		18	30		ns
Maximum Propagation Delay (Clear to Q)	$t_{PHL}, t_{PLH}$		21	30		ns
Maximum Removal Time (Clear to Clock)	$t_{REM}$		–1	5		ns
Minimum Set Up Time (D to Clock)	$t_S$		6	20		ns
Minimum Hold Time (Clock to D)	$t_H$		–3	5		ns
Minimum Pulse Width (Clock or Clear)	$t_W$		10	16		ns

**AC Electrical Characteristics:** ( $V_{CC} = 5V \pm 10\%$ ,  $t_r = t_f = 6\text{ns}$ ,  $C_L = 50\text{pF}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ \text{ to } +85^\circ\text{C}$		Unit
			Typ	Guaranteed Limits			
Maximum Operating Frequency	$f_{MAX}$		68	27	21		MHz
Maximum Propagation Delay (Clock to Q)	$t_{PHL}, t_{PLH}$		22	37	46		ns
Maximum Propagation Delay (Clear to Q)	$t_{PHL}, t_{PLH}$		25	35	44		ns
Minimum Removal Time (Clear to Clock)	$t_{REM}$		–1	5	6		ns
Minimum Setup Time (D to Clock)	$t_S$		6	20	25		ns
Minimum Hold Time (Clock to D)	$t_H$		–3	5	5		ns
Minimum Pulse Width (Clock or Clear)	$t_W$		10	16	25		ns
Maximum Input Rise and Fall Time (Clock)	$t_r, t_f$		–	500	500		ns
Maximum Output Rise and Fall Time	$t_{THL}, t_{TLH}$		11	15	19		ns
Power Dissipation Capacitance	$C_{PD}$	Per Flip-Flop, Note 5	–	–	–		pF
Maximum Input Capacitance	$C_{IN}$		6	10	10		pF

Note 5.  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC}^2 f + I_{CC}$ .

**Truth Table:** (Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

H = High Level (Steady-State)

L = Low Level (Steady-State)

X = Don't Care

↑ = Transition from Low-to-High Level

Q0 = The level of Q before the indicated steady-state input conditions were established.

**Pin Connection Diagram**



