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NTE74S194
Integrated Circuit
TTL – 4–Bit Bidirectional Universal Shift Register

Description:

The NTE74S194 is a 4–bit bidirectional shift register in a 16–Lead plastic DIP type package designed to incorporate virtually all of the features a system designer may want is a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right–shift and left–shift serial inputs, operating–mode–control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Inhibit Clock (Do Nothing)
Shift Right (In the Direction Q_A Toward Q_D)
Shift Left (In the Direction Q_D Toward Q_A)
Parallel (Broadside) Load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip–flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift–right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift–left serial input.

Clocking of the shift register is inhibited when both control inputs are low.

Features:

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge–Triggered Clock
- Direct Overriding Clear

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 5.5V
Power Dissipation, P_D 425mW
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Output Current	I_{OH}	–	–	−1	mA
Low−Level Output Current	I_{OL}	–	–	20	mA
Clock Frequency	f_{clock}	0	–	70	MHz
Width of Clock Pulse	$t_{w(clock)}$	7	–	–	ns
Width of Clear Pulse	$t_{w(clear)}$	12	–	–	ns
Mode Control Setup Time	t_{su}	11	–	–	ns
Serial and Parallel Data Setup Time	t_{su}	5	–	–	ns
Clear Inactive−State Setup Time	t_{su}	9	–	–	ns
Hold Time at Any Input	t_h	3	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High−Level Input Voltage	V_{IH}		2	–	–	V
Low−Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA	–	–	−1.2	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1mA	2.7	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20mA	–	–	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.7V	–	–	50	μA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.5V	–	–	−2	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4	−40	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5	–	85	135	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. Not more than one output should be shorted at a time and duration of short−circuit should not exceed one second.

Note 5. With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, clear, and the serial inputs, I_{CC} is measured with momentary GND, then 4.5V applied to clock.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	R_L = 280Ω, C_L = 15pF	70	105	–	MHz
Propagation Delay Time (from Clear)	t_{PHL}		–	12.5	18.5	ns
Propagation Delay Time (from Clock)	t_{PLH}		4	8	12	ns
	t_{PHL}		4	11	16.5	ns

Function Table:

Inputs										Outputs			
	Mode			Serial		Parallel							
Clear	S1	S0	Clock	Left	Right	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = HIGH Level (Steady State)

L = LOW Level (Steady State)

X = Irrelevant (Any input, including transitional)

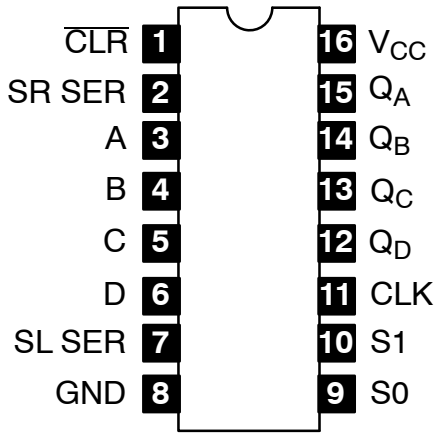
↑ = Transition from LOW to HIGH Level

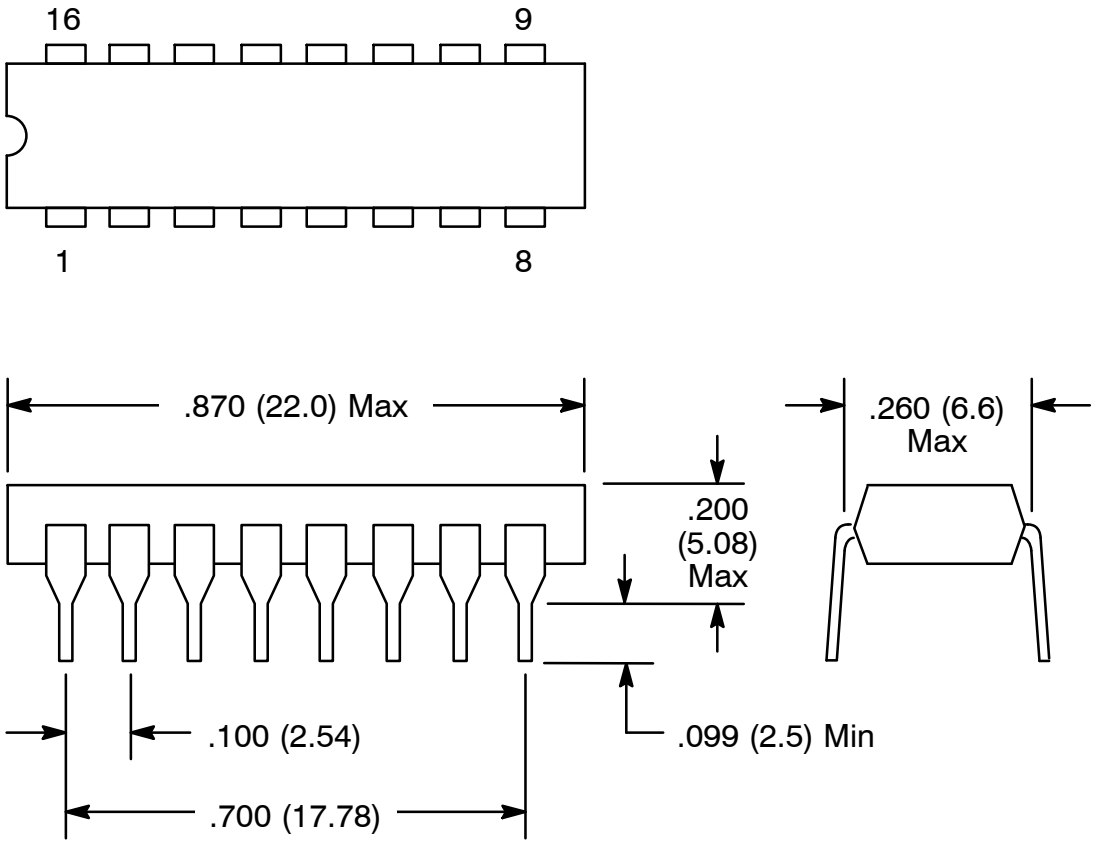
a, b, c, d = The level of steady−state input at inputs A, B, C, or D respectively

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D respectively, before the indicated steady−state input conditions were established

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C respectively, before the most recent ↑ transition of the clock.

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)