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NTE75188
Integrated Circuit
Diode Transistor Logic (DTL)
Quad Line Driver

Description:

The NTE75188 is a monolithic quadruple line driver in a 14–Lead DIP type package designed to interface data terminal equipment with data communications equipment in conformance with EIA Standard RS–232–C using a diode in series with each supply–voltage terminal.

Features:

- Meets Specifications of EIA RS–232–C
- Current–Limited Output: 10mA Typ
- Power–Off Output Impedance: 300Ω Min
- Slew Rate Control by Load Capacitor
- Flexible Supply Voltage Range
- Input Compatible with Most TTL Circuits

Absolute Maximum Ratings: (T_A = 0 to +70°C unless otherwise specified)

Supply Voltage ($T_A \le$ +25°C, Note 1)

V_{CC} . . . . . +15V

V_{EE} . . . . . –15V

Input Voltage Range . . . . . –15V to +7V

Output Voltage Range . . . . . –15V to +15V

Continuous Total Dissipation ($T_A \le$ +25°C), P_D 1025mW

Operating Ambient Temperature range, T_A . . . . . 0 to +70°C

Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Lead Temperature (During Soldering 1/16” (1.6mm) from case, 60sec Max), T_L . . . . . +300°C

Note 1. All voltage values are with respect to the network GND pin.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	7.5	9.0	15.0	V
	V_{EE}	–7.5	–9.0	–15.0	V
High Level Input Voltage	V_{IH}	1.9	–	–	V
Low Levev Input Voltage	V_{IL}	–	–	0.8	V
Operating Ambient Temperature	T_A	0	–	+70	°C

Electrical Characteristics: (T_A = 0 to +70°C, V_{CC} = 9V, V_{EE} = −9V unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
High Level Output Voltage	V_{OH}	V_{IL} = 800mV, R_L = 3kΩ	V_{CC} = 9V, V_{EE} = −9V	6	7	–	V
			V_{CC} = 13.2V, V_{EE} = −13.2V	9.0	10.5	–	V
Low Level Output Voltage	V_{OL}	V_{IH} = 1.9V, R_L = 3kΩ	V_{CC} = 9V, V_{EE} = −9V	–	−7	−6	V
			V_{CC} = 13.2V, V_{EE} = −13.2V	–	−10.5	−9.0	V
High Level Input Current	I_{IH}	V_I = 5V		–	–	10	μA
Low Level Input Current	I_{IL}	V_I = 0		–	−1.0	−1.6	mA
Short Circuit Output Current at High Level	$I_{OS(H)}$	V_I = 800mV, V_O = 0, Note 3		−6	−9	−12	mA
Short Circuit Output Current at Low Level	$I_{OS(L)}$	V_I = 1.9V, V_O = 0, Note 3		6	9	12	mA
Output Resistance, Power Off	r_o	V_{CC} = 0, V_{EE} = 0, V_O = −2V to +2V		300	–	–	Ω
Supply Current from V_{CC}	I_{CC}	V_{CC} = 9V, No Load	All Inputs at 1.9V	–	15	20	mA
			All Inputs at 800mV	–	4.5	6.0	mA
		V_{CC} = 12V, No Load	All Inputs at 1.9V	–	19	25	mA
			All Inputs at 800mV	–	5.5	7.0	mA
		V_{CC} = 15V, No Load, T_A = +25°C	All Inputs at 1.9V	–	–	34	mA
			All Inputs at 800mV	–	–	12	mA
Supply Current from V_{EE}	I_{EE}	V_{EE} = −9V, No Load	All Inputs at 1.9V	–	−13	−17	mA
			All Inputs at 800mV	–	–	−0.015	mA
		V_{EE} = −12V, No Load	All Inputs at 1.9V	–	−18	−23	mA
			All Inputs at 800mV	–	–	−0.015	mA
		V_{EE} = −15V, No Load, T_A = +25°C	All Inputs at 1.9V	–	–	−34	mA
			All Inputs at 800mV	–	–	−2.5	mA
Total Power Dissipation	P_D	V_{CC} = 9V, V_{EE} = −9V, No Load		–	–	333	mW
		V_{CC} = 12V, V_{EE} = −12V, No Load		–	–	576	mW

Note 2. All typical values are at T_A = +25°C.
Note 3. Not more than one output should be shorted at a time.
Note 4. The algebraic convention in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only, e.g., if −6V is a maximum, the typical value is a more negative voltage.

Switching Characteristics: (T_A = +25°C, V_{CC} = 9V, V_{EE} = −9V unless otherwise specified)

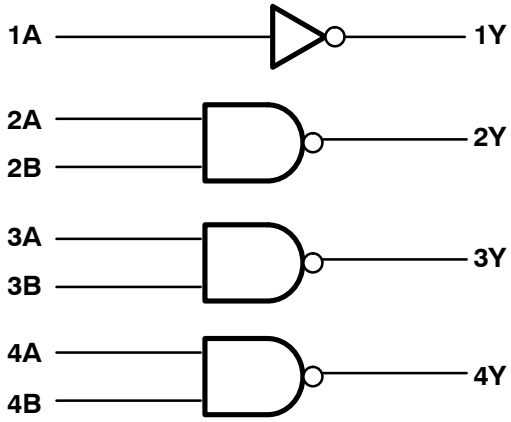
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Propagation Delay Time, Low–to–High–Level Output	t_{PLH}	R_L = 3kΩ, C_L = 15pF		–	220	350	ns
Propagation Delay Time, High–to–Low–Level Output	t_{PHL}			–	100	175	ns
Transition Time, Low–to–High Level Output	t_{TLH}		Note 5	–	55	100	ns
Transition Time, High–to–Low Level Output	t_{THL}		Note 5	–	45	75	ns
Transition Time, Low–to–High Level Output	t_{TLH}	R_L = 3kΩ to 7kΩ, C_L = 2500pF, Note 6		–	2.5	–	ns
Transition Time, High–to–Low Level Output	t_{THL}			–	3.0	–	ns

Note 5. Measured between 10% and 90% points of output waveform.
Note 6. Measured between +3V and −3V points on the output waveform.

Function Table:
(Drivers 2 thru 4)

A	B	Y
H	H	L
L	X	H
X	L	H

Logic Diagram
(Positive Logic)



Positive Logic
$Y = \overline{A}$ (Driver 1)
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$ (Drivers 2 thru 4)

Pin Connection Diagram