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NTE8542
Integrated Circuit
Tri–State Quad I/O Register

General Description:

The NTE8542 is a 4–bit storage register with two terminals per bit which may be used as either inputs or outputs when tied to two bus lines. Storage capability is obtained with positive edge triggered flip–flops having common clock and asynchronous clear. Each I/O terminal can be forced to a high impedance state (Hi–z state) using the Output Disable controls.

Features:

- Series 54/74 compatible
- Input clamp diodes
- Propagation delays 25ns
- Power dissipation 400mW
- Operation 40MHz

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7.0V
Input Voltage, V_i 5.5V
Output Voltage, V_O 5.5V
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

Recommended Operating Conditions:

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.75	5.25	V
Temperature	T_A	0	+70	°C

Note 1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. Except for “Operating Temperature Range” they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

Electrical Characteristics: (Notes 2 and 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Logical “1” Input Voltage	V_{IH}	V_{CC} = Min	2.0	–	–	V
Logical “1” Input Current	I_{IH}	V_{CC} = Max, V_{IN} = 2.4V V_{CC} = Max, V_{IN} = 5.5V	– –	– –	40 1.0	μA
Logical “0” Input Voltage	V_{IL}	V_{CC} = Min	–	–	0.8	V
Logical “0” Input Current	I_{IL}	V_{CC} = Max, V_{IN} = 0.4V	–	–1.0	–1.6	mA
Input Clamp Voltage	V_{CD}	V_{CC} = Min, I_{IN} = –12mA	–	–	–1.5	V
Logical “1” Output Voltage	V_{OH}	V_{CC} = Min, I_{OUT} = –800μ	2.4	–	–	V
Output Short Circuit Current	I_{OS}	V_{CC} = Max, V_{OUT} = 0V, Note 4	–25	–	–70	mA
Logical “0” Output Voltage	V_{OL}	V_{CC} = Min, I_{OUT} = 16mA	–	–	0.4	V
Supply Current	I_{CC}	V_{CC} = Max	–	–	120	mA
TRI–STATE I/O Current with Inputs and Outputs Disabled		V_{CC} = Max, V_{IN} = 2.4V V_{CC} = Max, V_{IN} = 0.4V	– –	– –	40 –40	μA
Propagation Delay to a Logical “0” from Clock to Output	t_{pd0}	R_L = 400Ω, C_L = 50pF T_A = 25°C	–	23	35	ns
Propagation Delay to a Logical “0” from Clear to Output	t_{pd0}	R_L = 400Ω, C_L = 50pF T_A = 25°C	–	24	36	ns
Propagation Delay to a Logical “1” from Clock to Output	t_{pd1}	R_L = 400Ω, C_L = 50pF T_A = 25°C	–	25	38	ns
Delay from Disable to High Impedance State (from Logical “1” Level)	t_{1H}	R_L = 400Ω, C_L = 5.0pF T_A = 25°C	–	6.0	15	ns
Delay from Disable to High Impedance State (from Logical “0” Level)	t_{0H}	R_L = 400Ω, C_L = 5.0pF T_A = 25°C	–	15	25	ns
Delay from Disable to Logical “1” Level (from High Impedance State)	t_{H1}	R_L = 400Ω, C_L = 50pF T_A = 25°C	–	20	30	ns
Delay from Disable to Logical “0” Level (from High Impedance State)	t_{H0}	R_L = 400Ω, C_L = 50pF T_A = 25°C	–	17	25	ns
Maximum Clock Frequency	f_{MAX}	R_L = 400Ω, C_L = 50pF T_A = 25°C	30	40	–	MHz
Enable to Clock Set–Up Time	t_{SO}	R_L = 400Ω, C_L = 50pF T_A = 25°C	20	13	–	ns
Enable to Clock Set–Up Time	t_{SI}	R_L = 400Ω, C_L = 50pF T_A = 25°C	20	12	–	ns

Electrical Characteristics (Cont'd): (Notes 2 and 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Date to Clock Set−Up Time	t_{SO}	R_L = 400Ω, C_L = 50pF T_A = 25°C	10	4.5	–	ns
Date to Clock Set−Up Time	t_{SI}	R_L = 400Ω, C_L = 50pF T_A = 25°C	5.0	−4.0	–	ns
Data to Clock Hold Time	t_{HO}	R_L = 400Ω, C_L = 50pF T_A = 25°	10	4.5	–	ns
Data to Clock Hold Time	t_{HI}	R_L = 400Ω, C_L = 50pF T_A = 25°C	5.0	−3.5	–	ns
Minimum Clock Pulse Width	PW_{MIN}	R_L = 400Ω, C_L = 50pF T_A = 25°C	20	–	–	ns
Minimum Clear Pulse Width	PW_{MIN}	R_L = 400Ω, C_L = 50pF T_A = 25°C	20	–	–	ns

Note 2. Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the NTE8542. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to GND unless otherwise noted. All values shown as max or min on absolute value basis.

MODE OF OPERATION:

CLEAR	DIS_1	DIS_2	$\overline{E}_1$	$\overline{E}_2$	A_{1-4}	B_{1-4}	Comments
0	0	1	1	1	Q	Hi−z	Output Data to Bus A
0	1	0	1	1	Hi−z	Q	Output Data to Bus B
0	0	0	1	1	Q	Q	Output Data to Both Buses
0	1	1	1	1	Hi−z	Hi−z	Store Data With Outputs in Hi−z State
0	X	X	0	1	Data	Q_N	Enter Data From Bus A
0	X	X	1	0	Q_N	Data	Enter Data From Bus B
0	X	X	0	0	Data	Data	Enter Data From Both Buses (Logic "1" on Either Will Dominate)
1	X	X	X	X	X	X	Clear

X = Don't Care State
Q_N = Data After Clock Transition

Pin Connection Diagram